

Fig.1 (Prior Art)

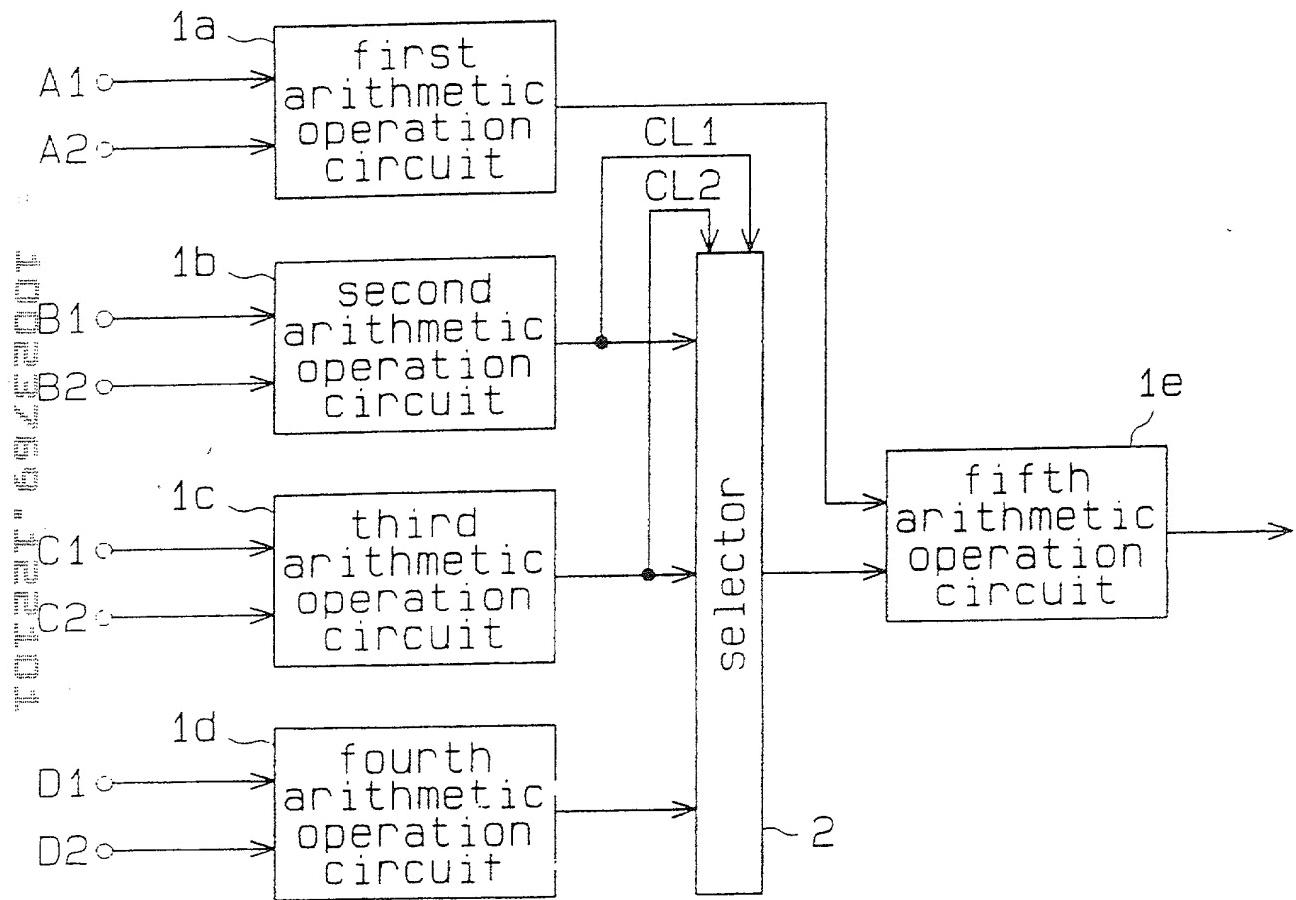
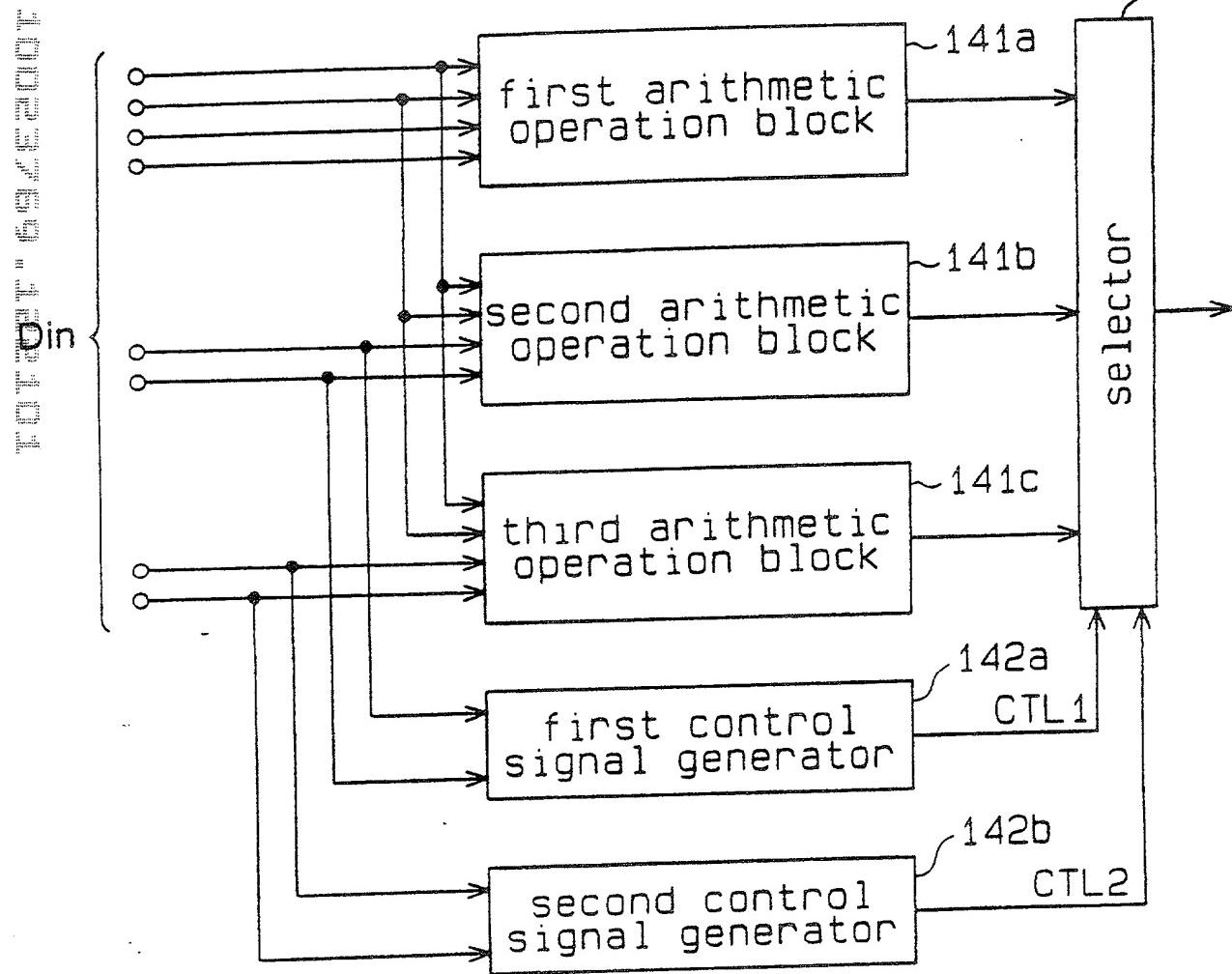


Fig.2



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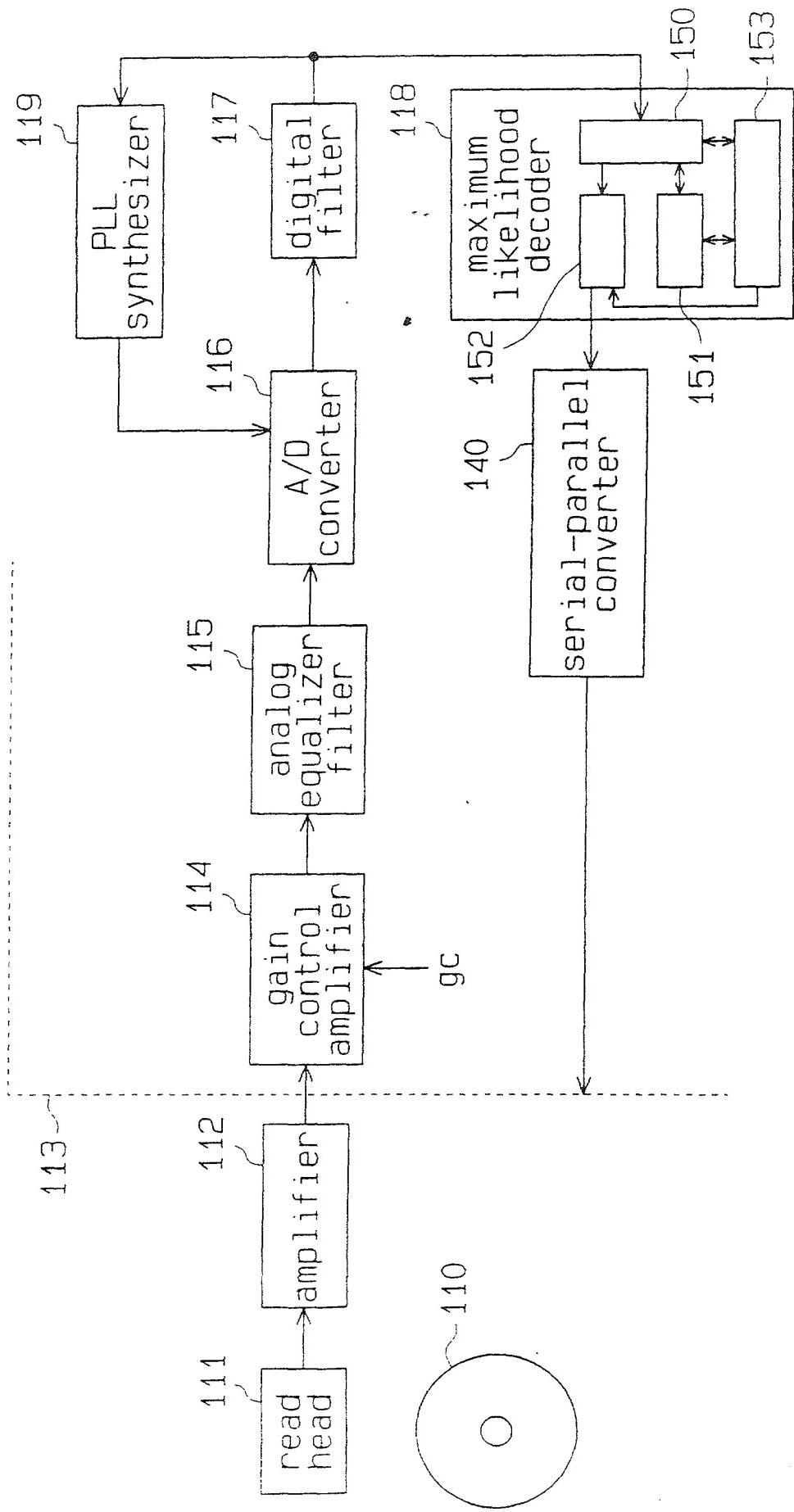


Fig. 4

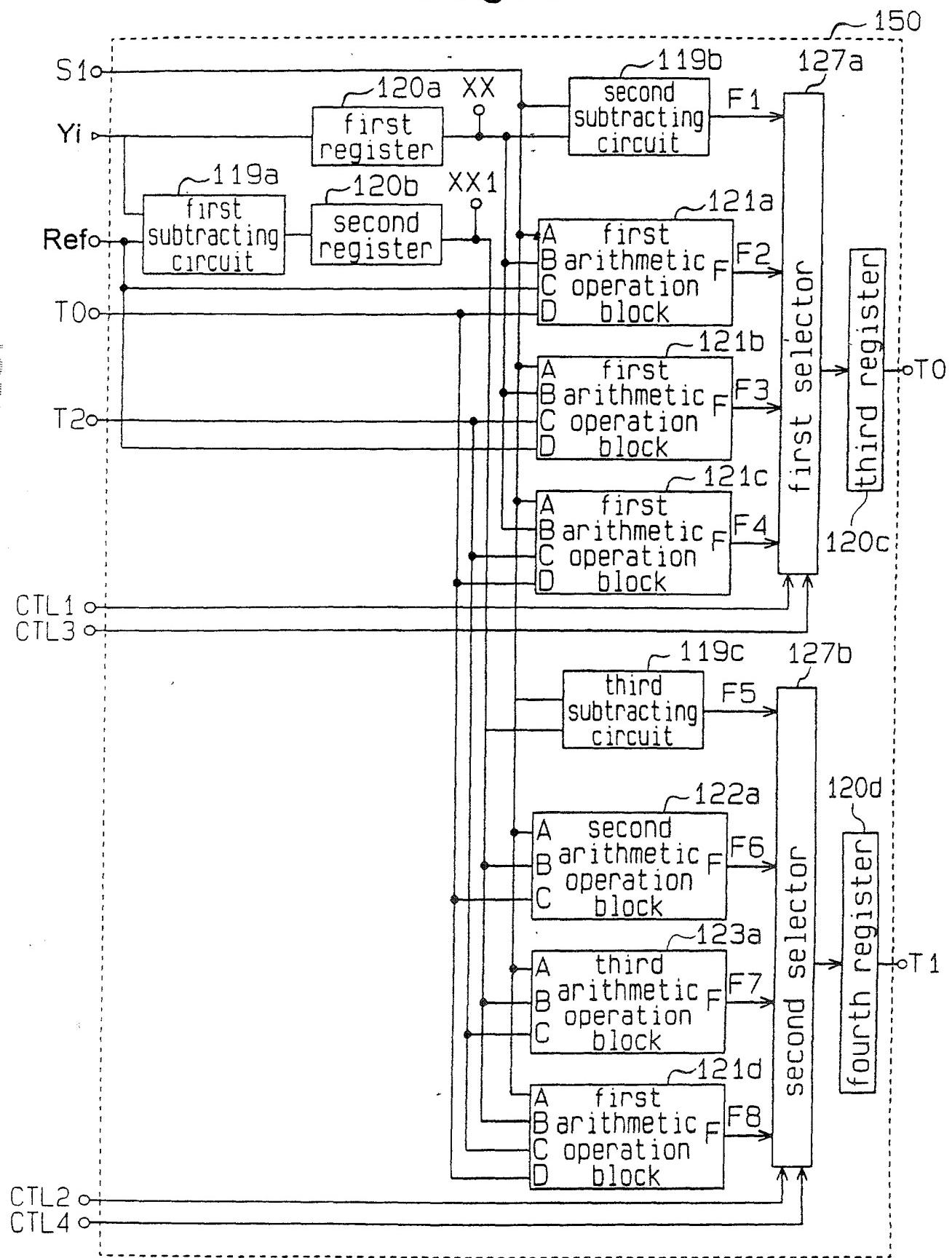


Fig. 5

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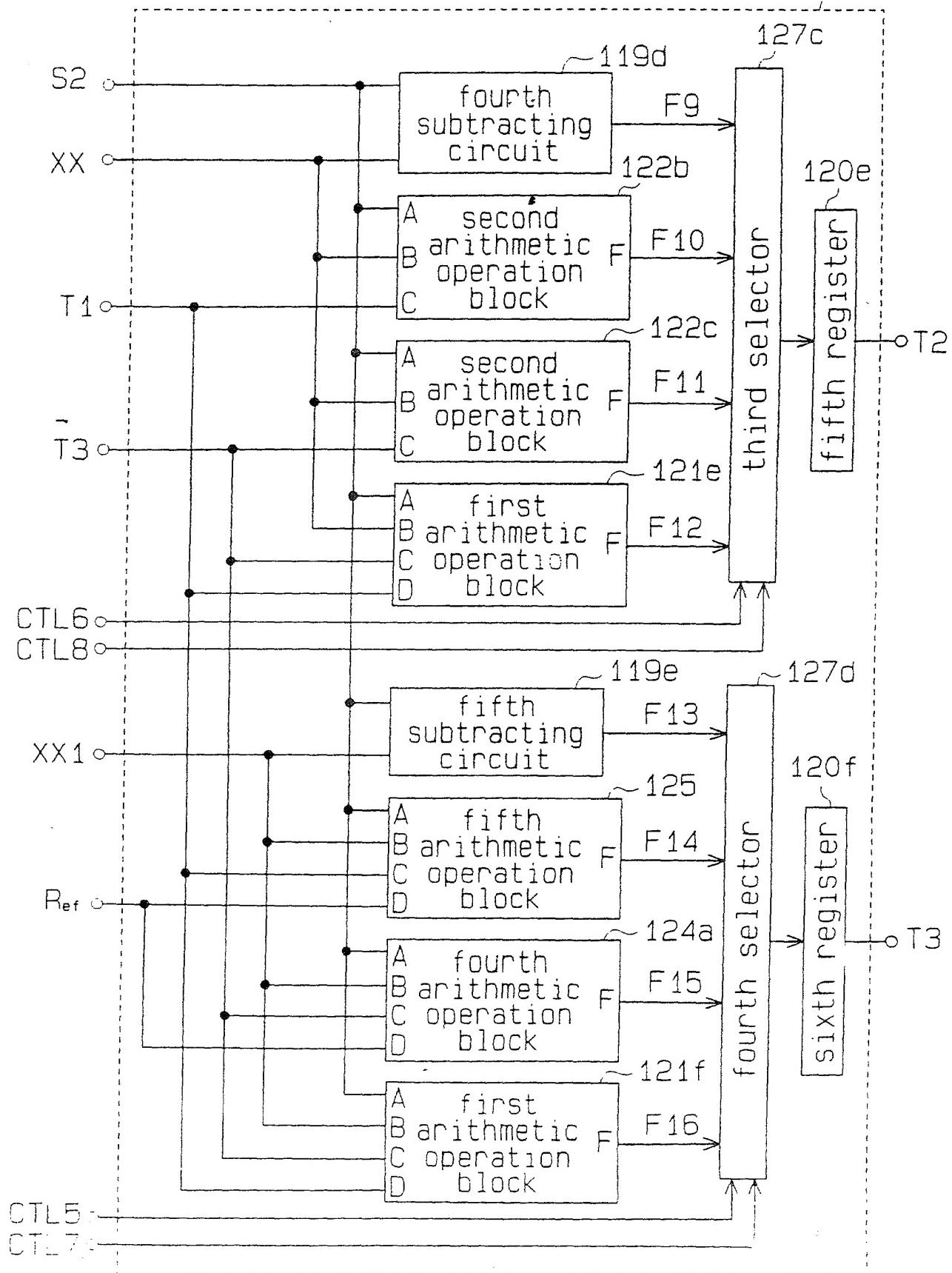


Fig.6

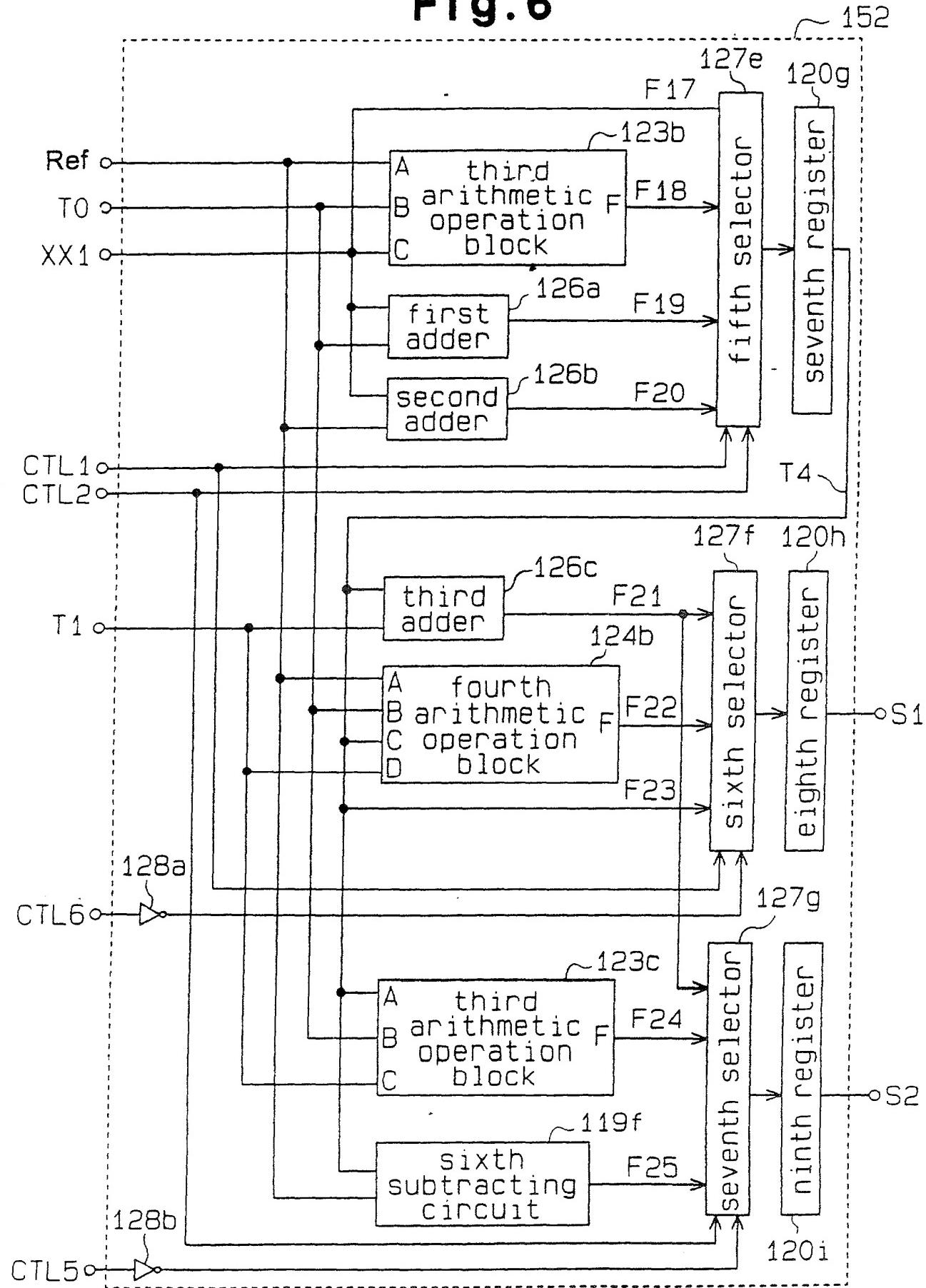


Fig. 7

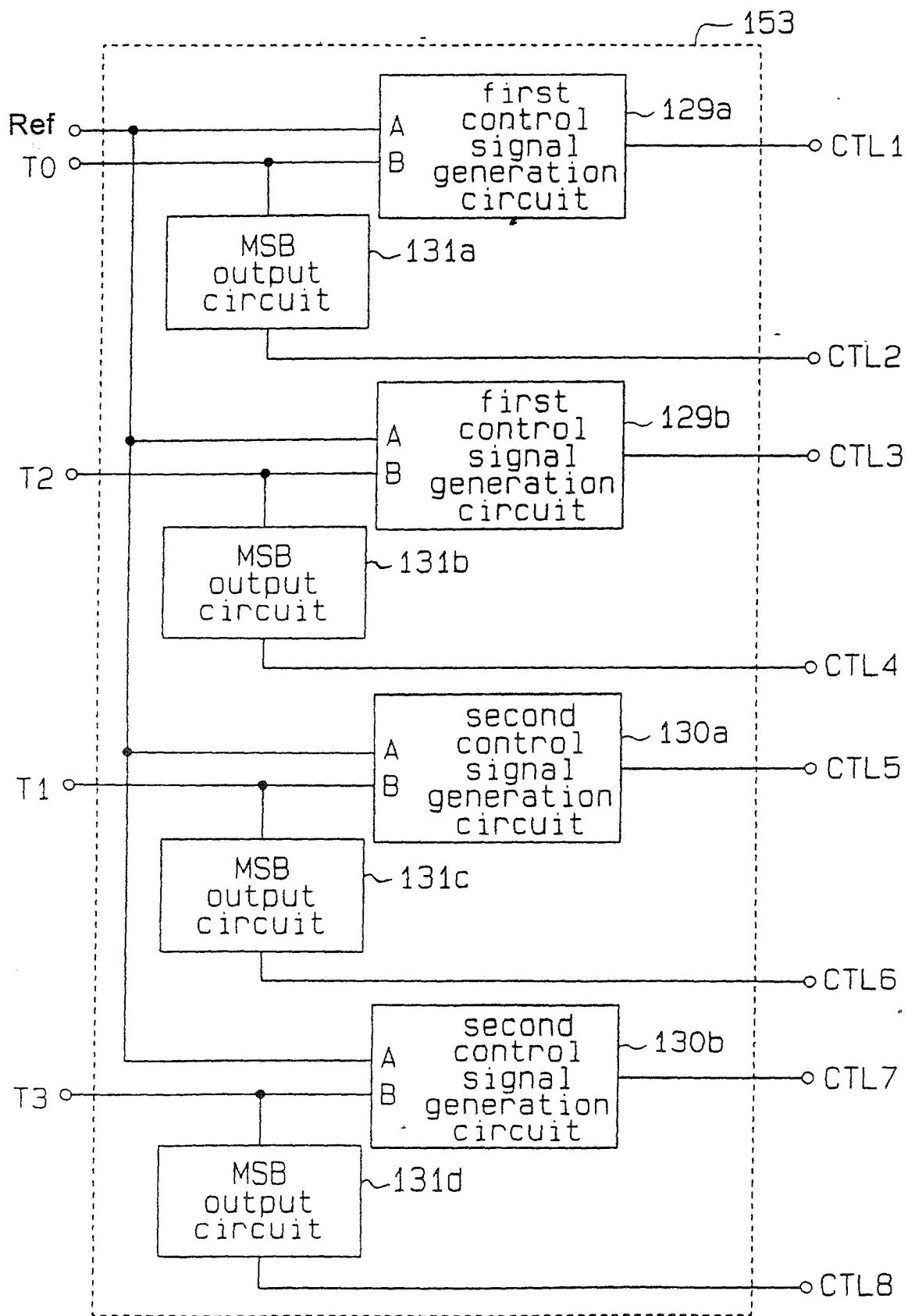
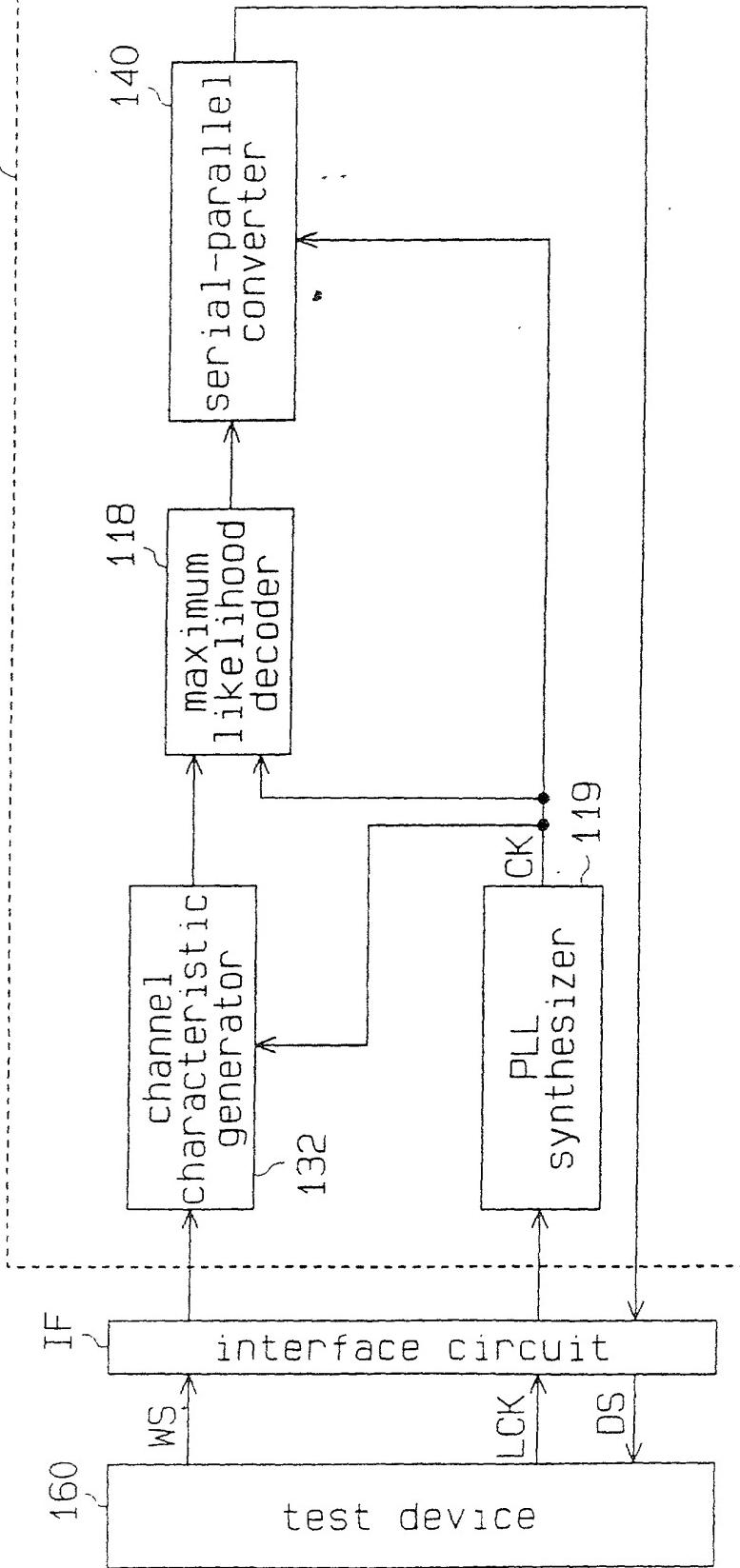


Fig. 8

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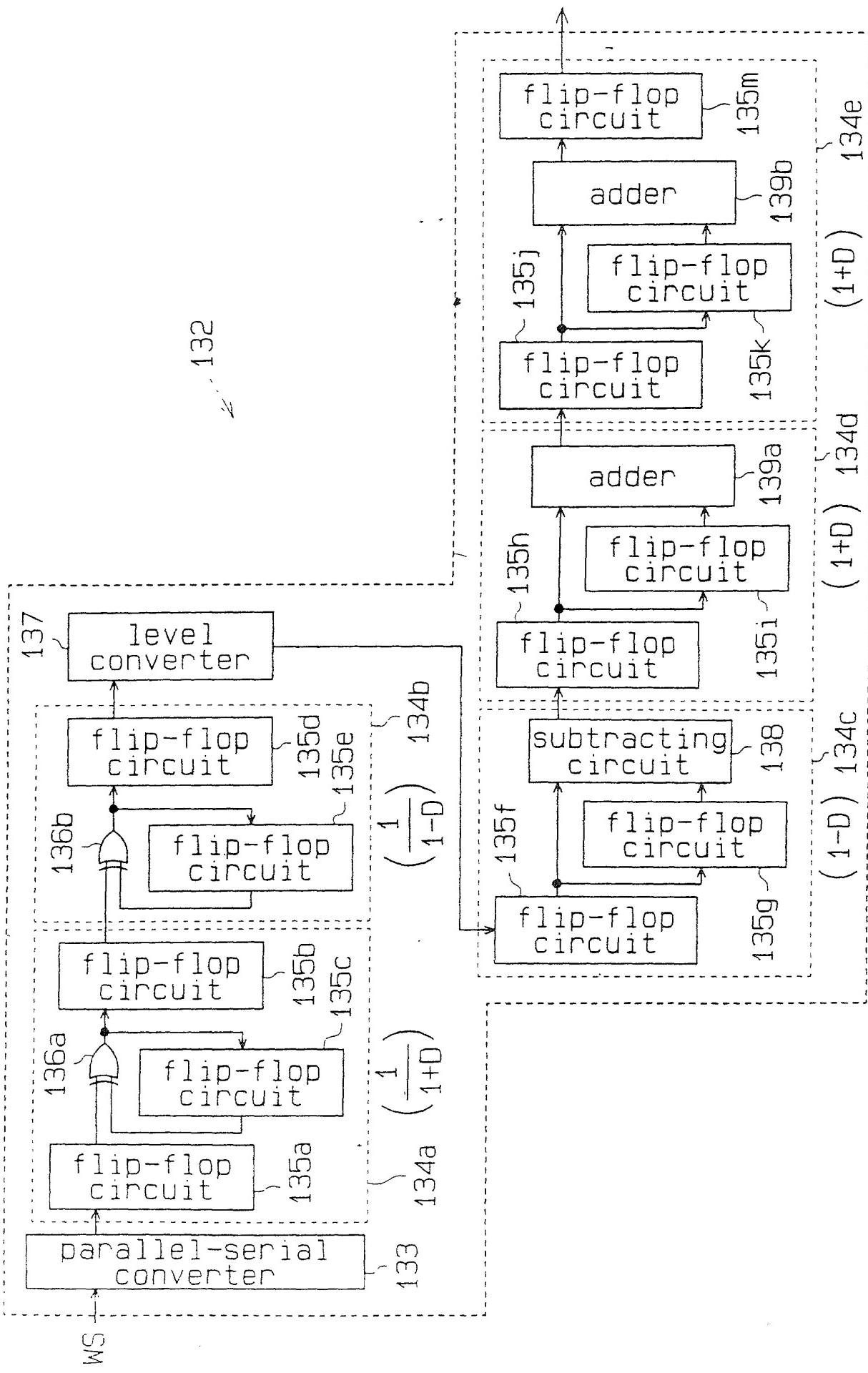


Fig.10

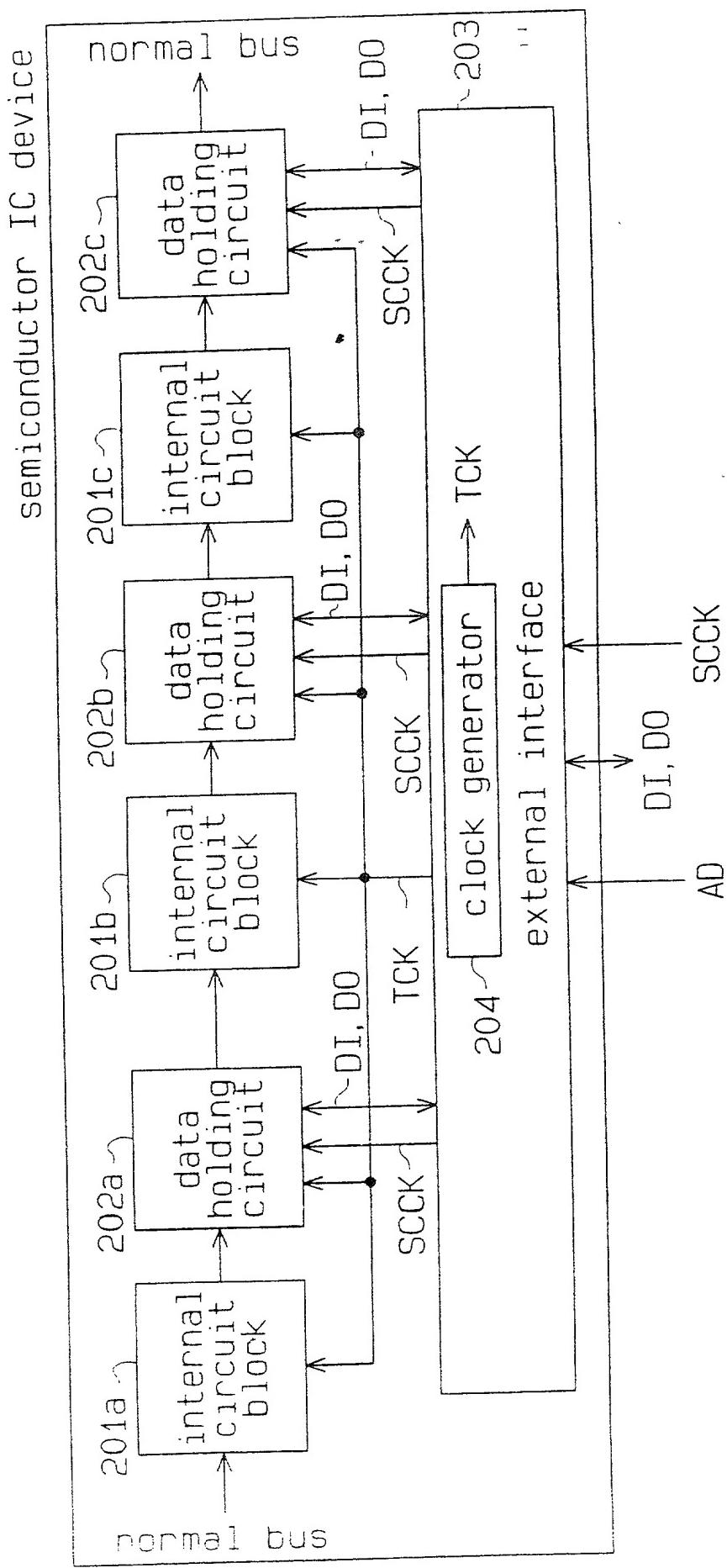


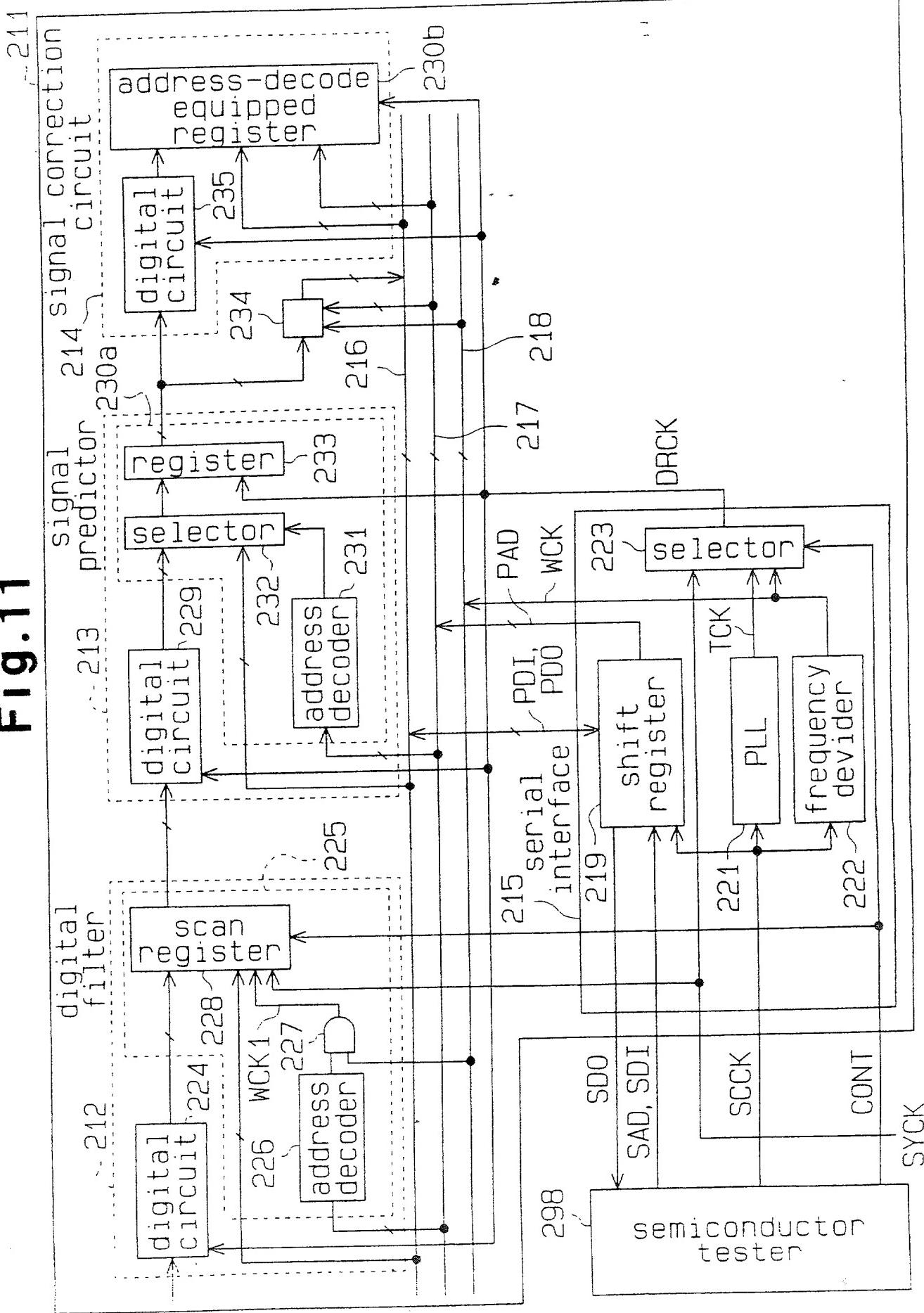
Fig. 11

Fig. 12

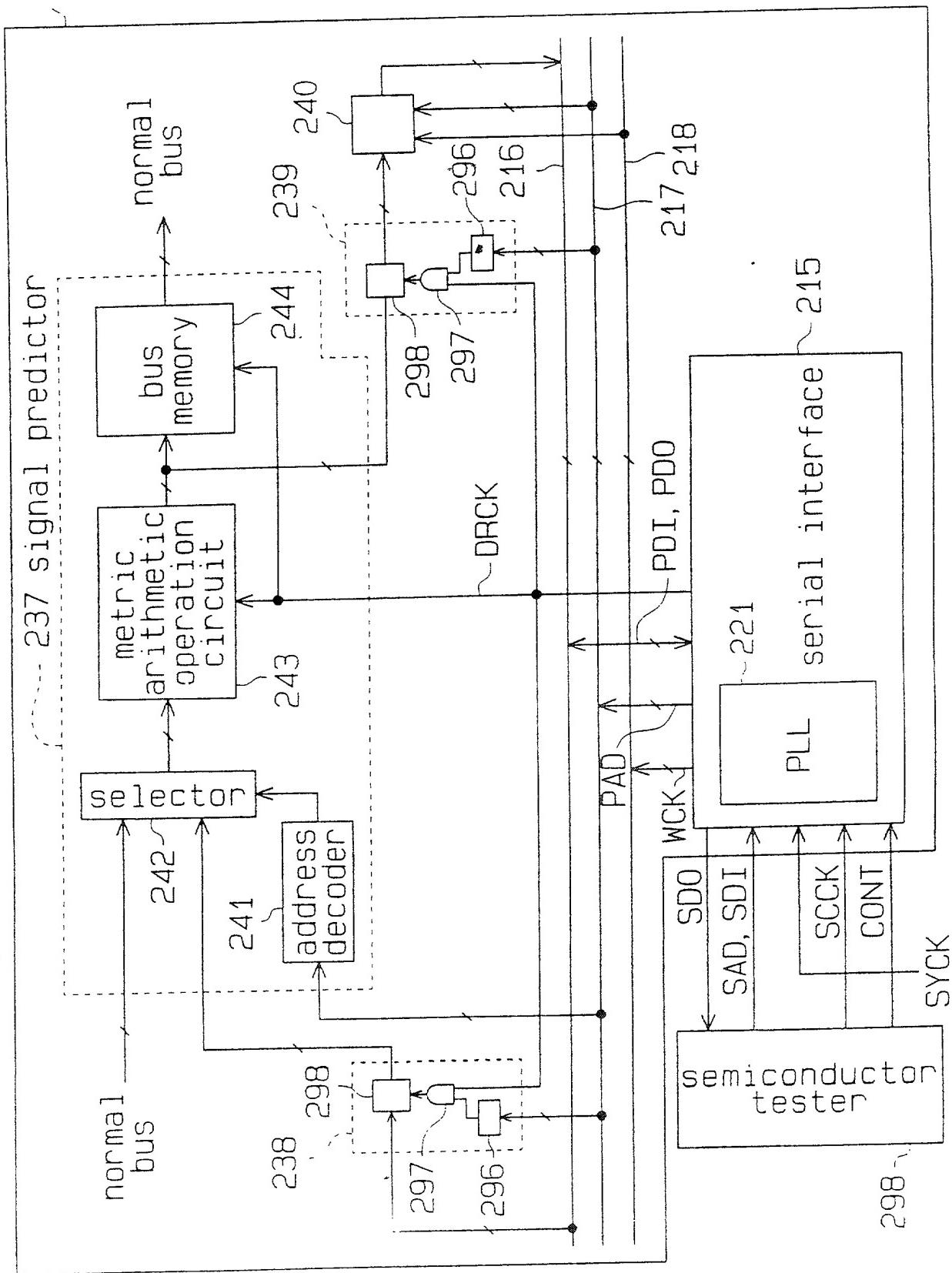


Fig. 13 *Block diagram of the test system*

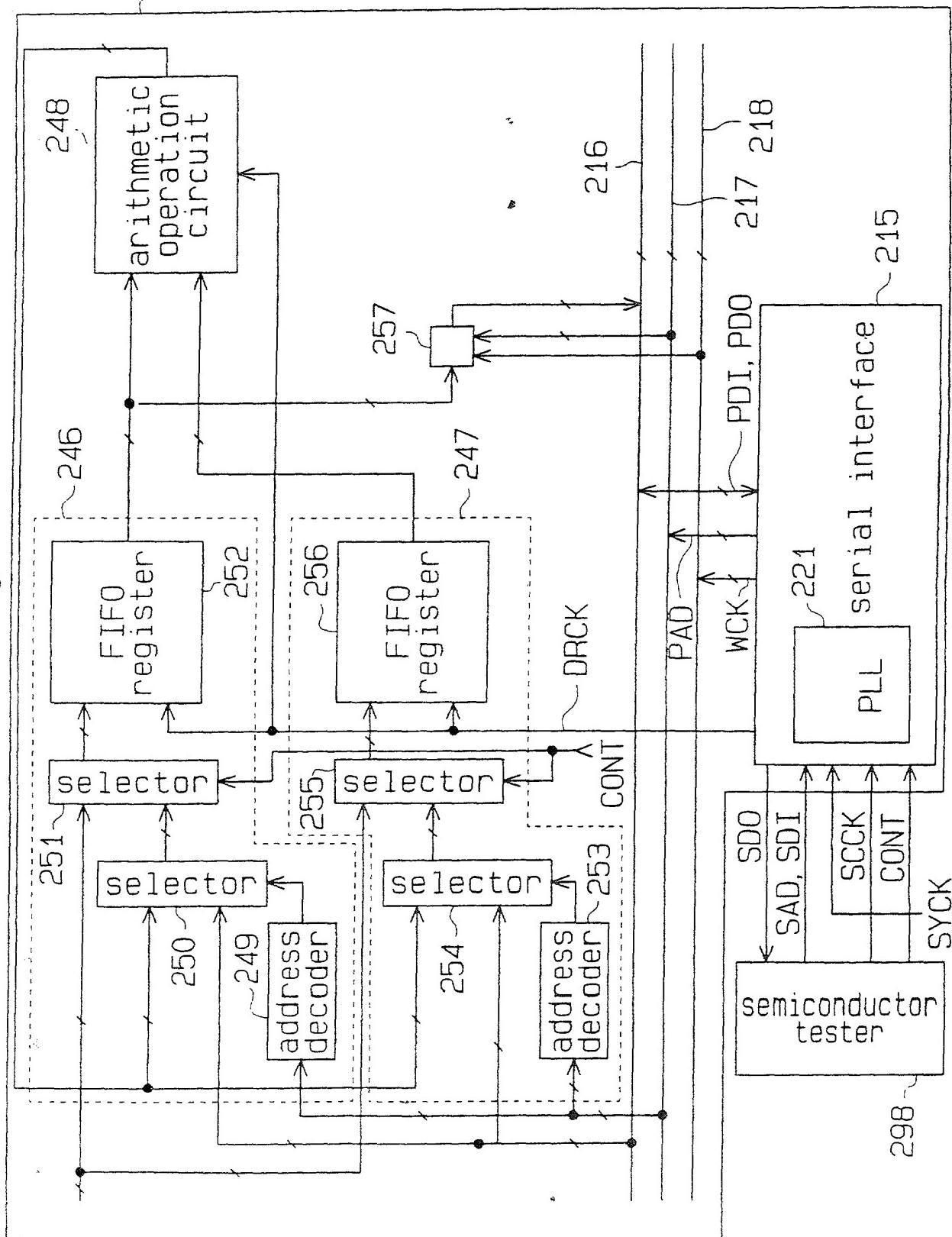


Fig. 14

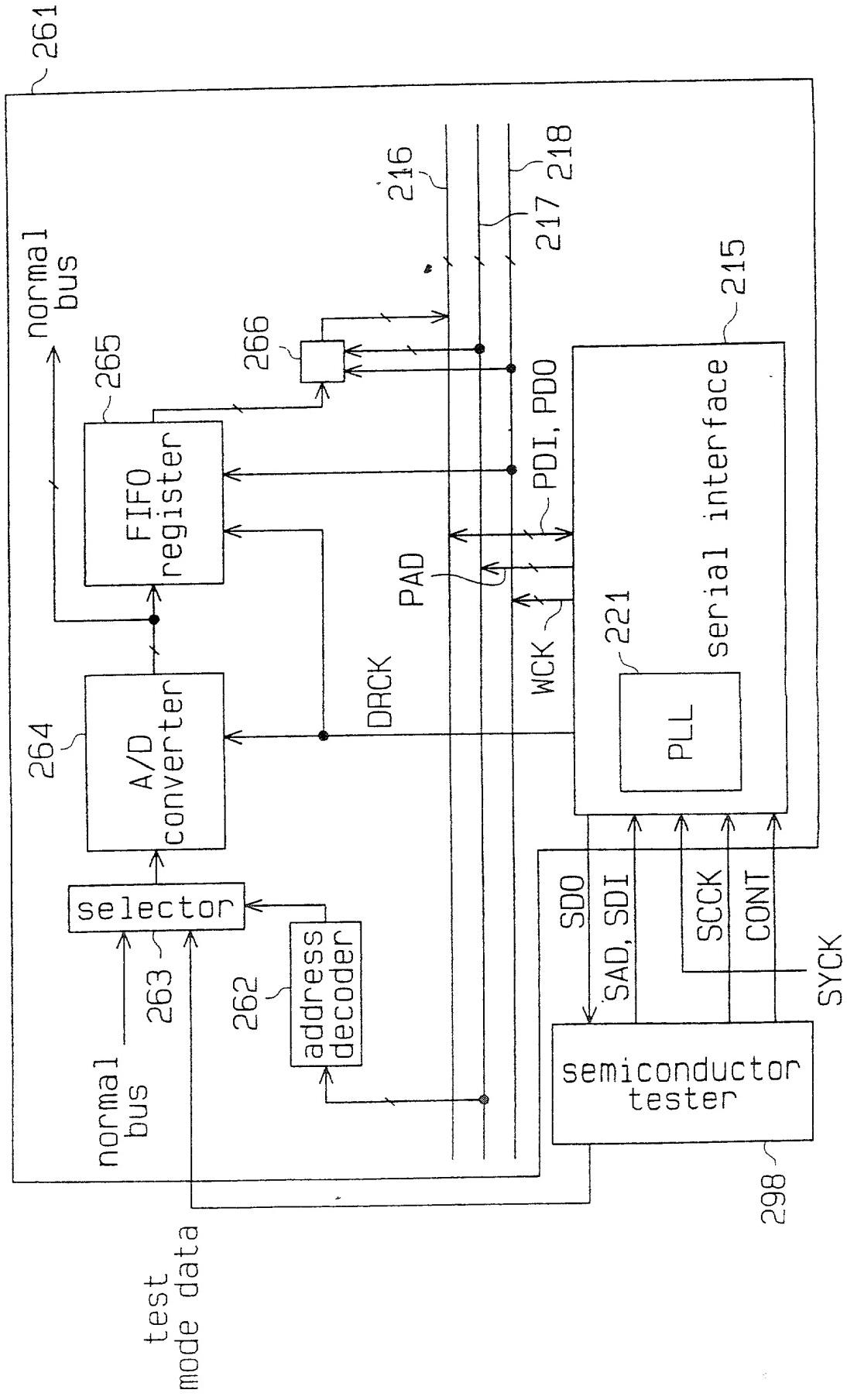
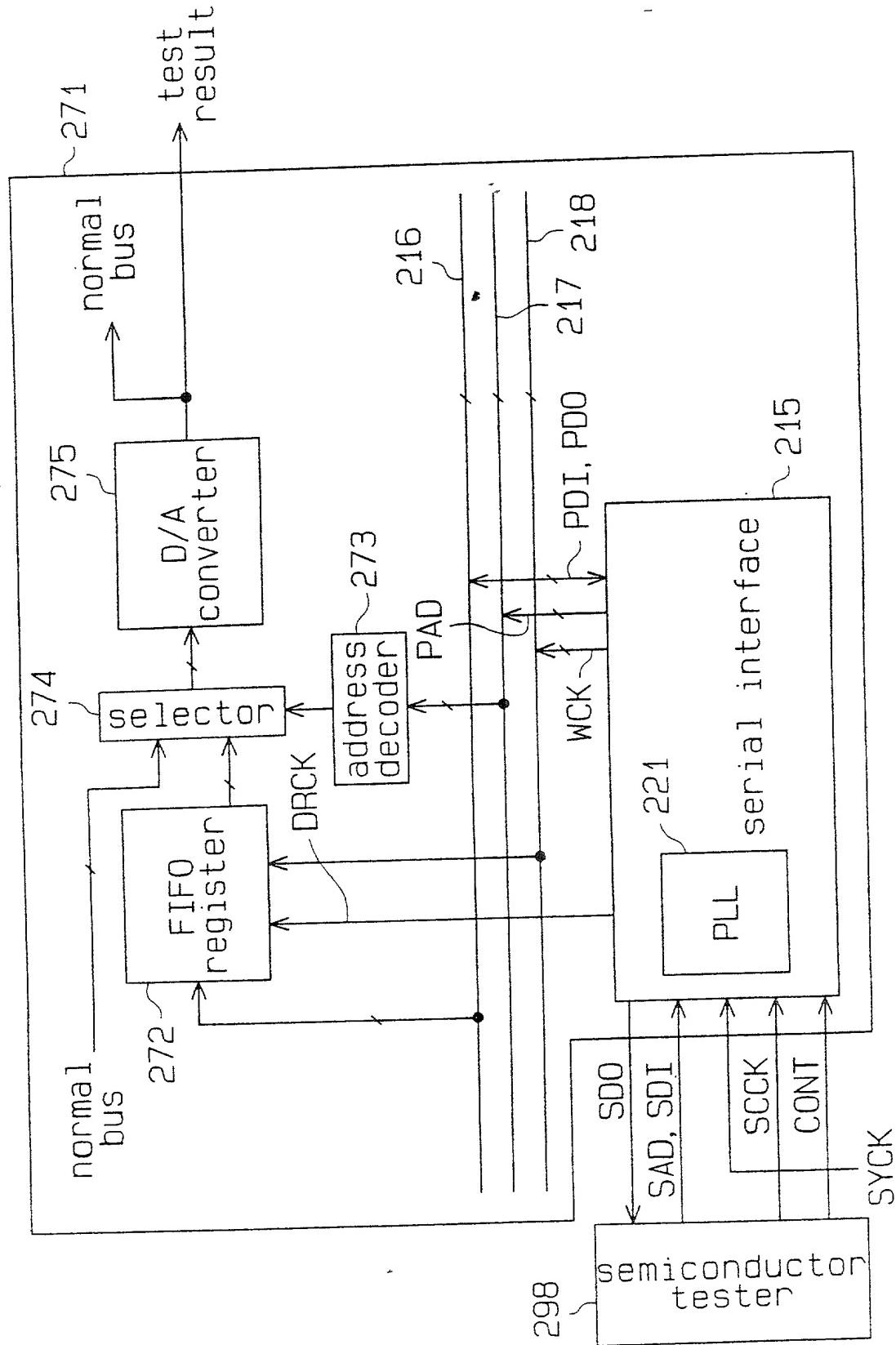
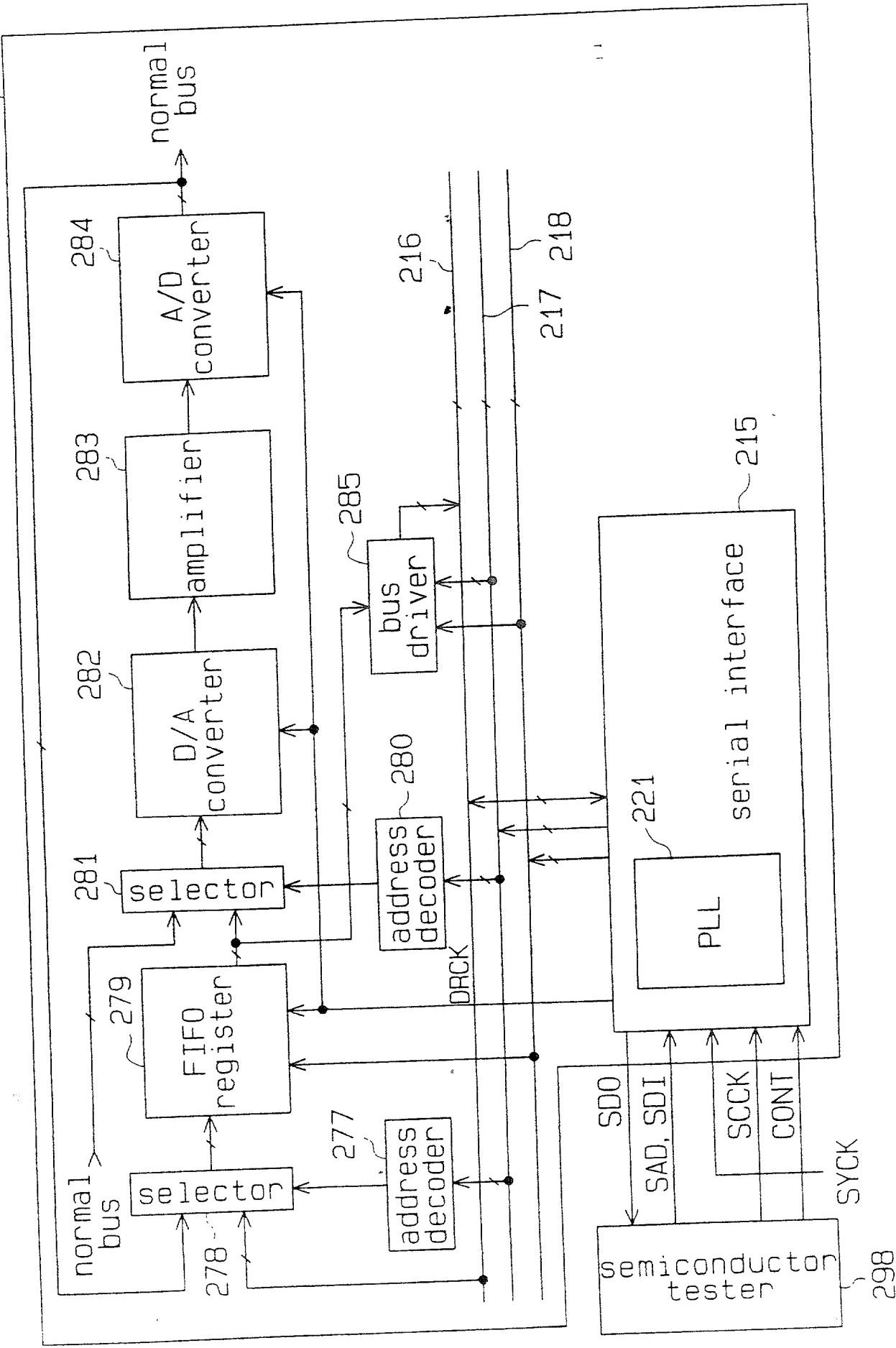


Fig. 15



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Fig. 16

298

Fig. 17

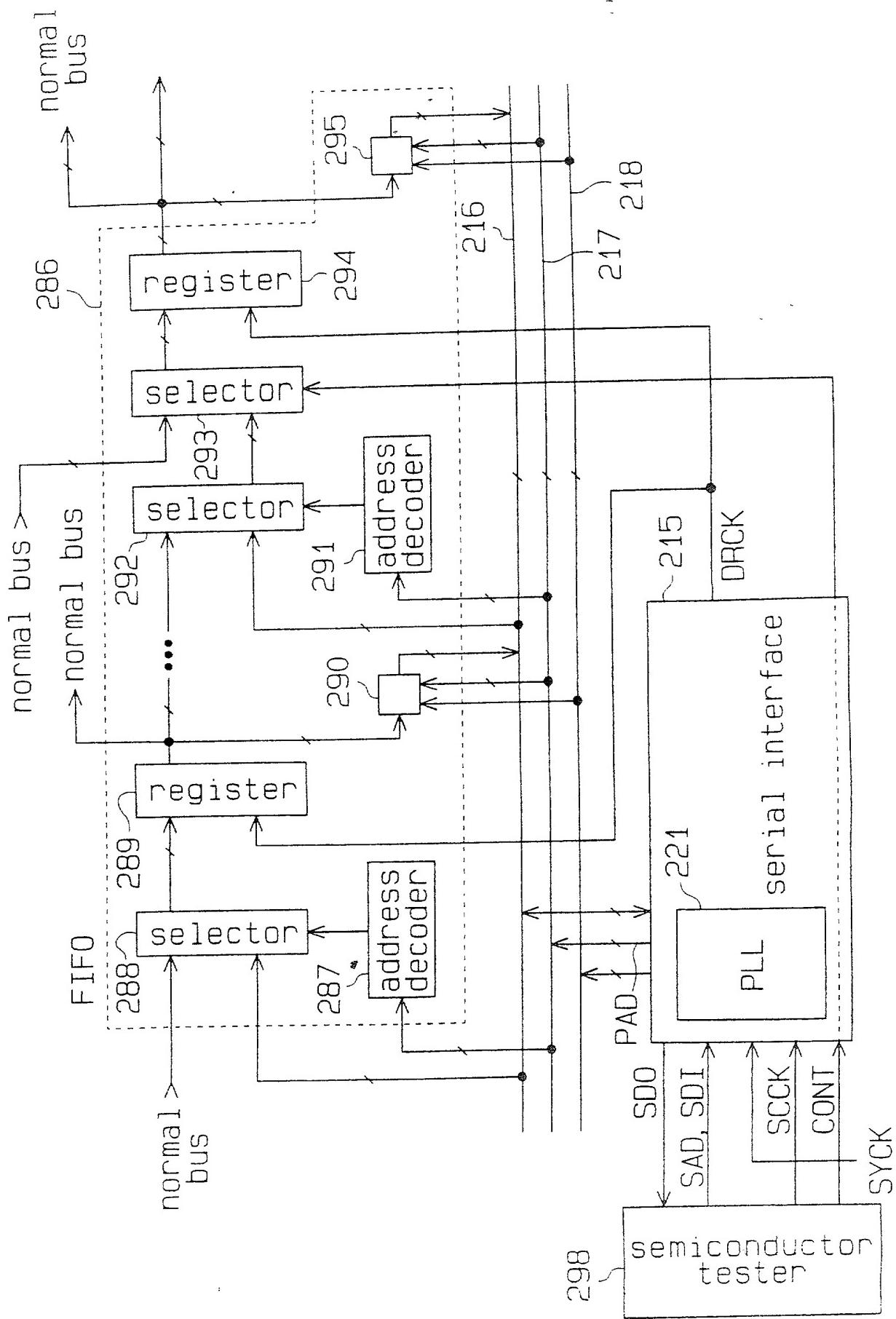


Fig. 18

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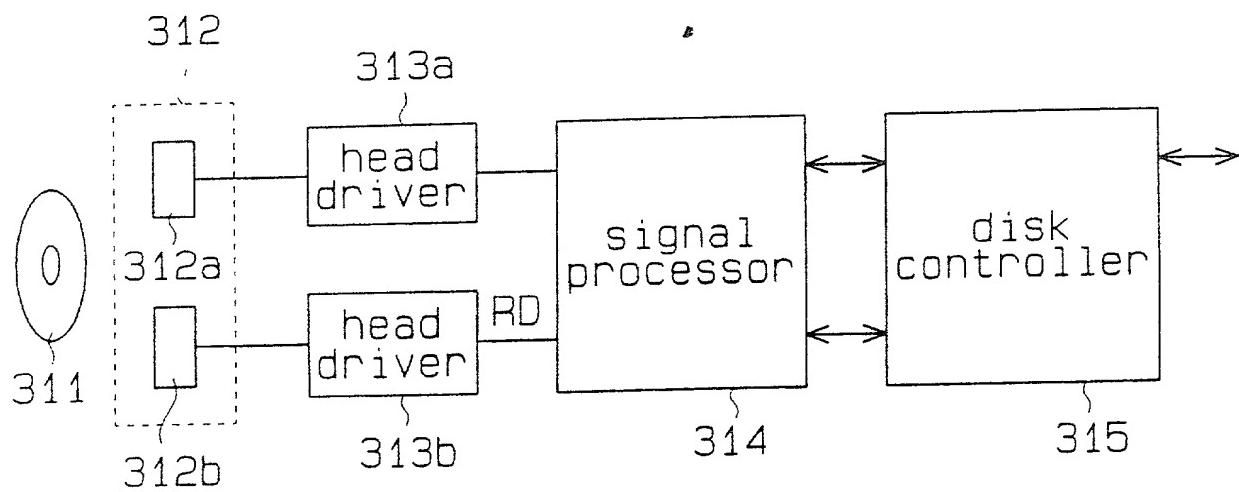


Fig. 19

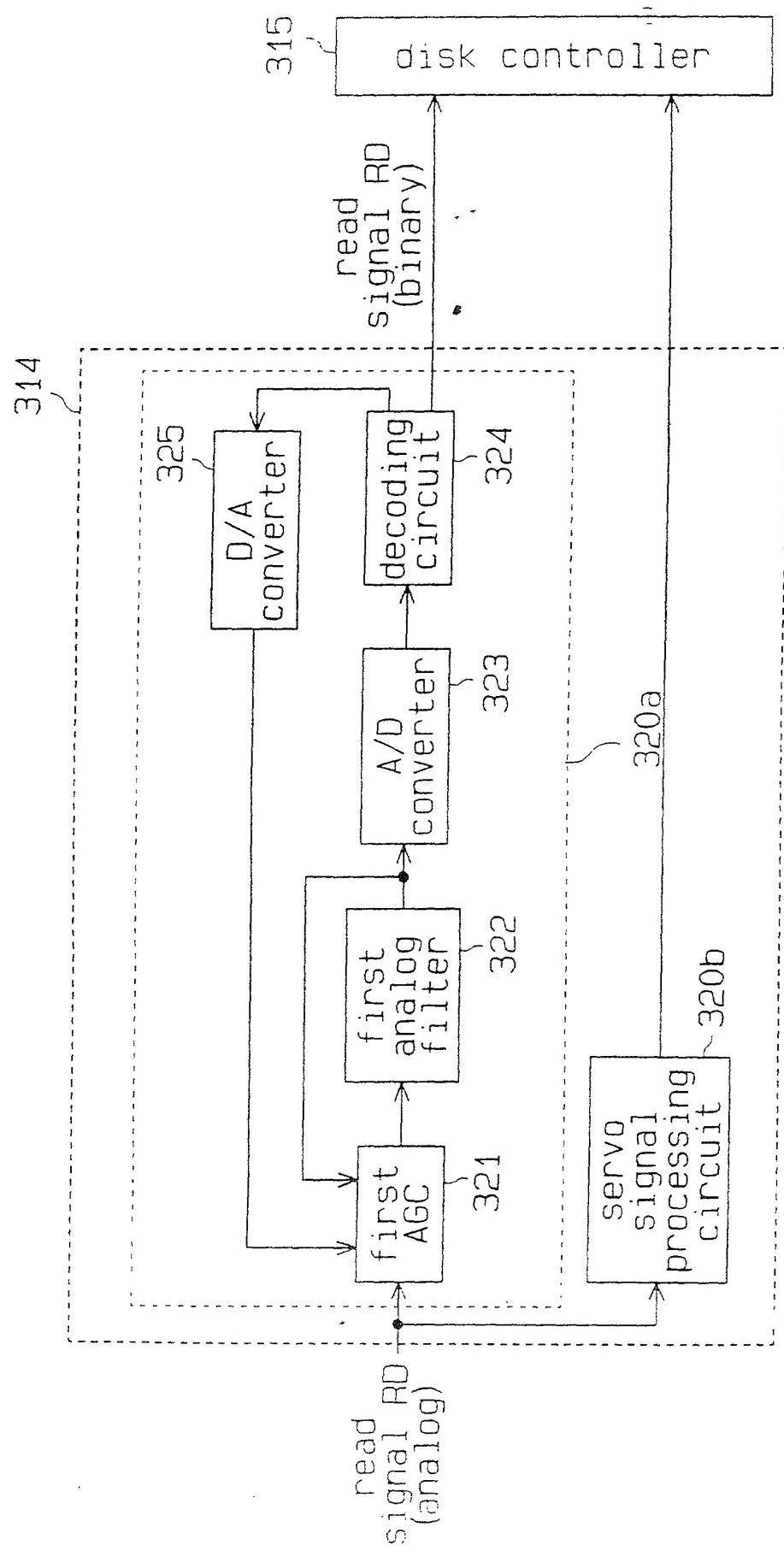


Fig. 20

Fig. 20 shows a detailed block diagram of a disk controller and associated signal processing circuitry.

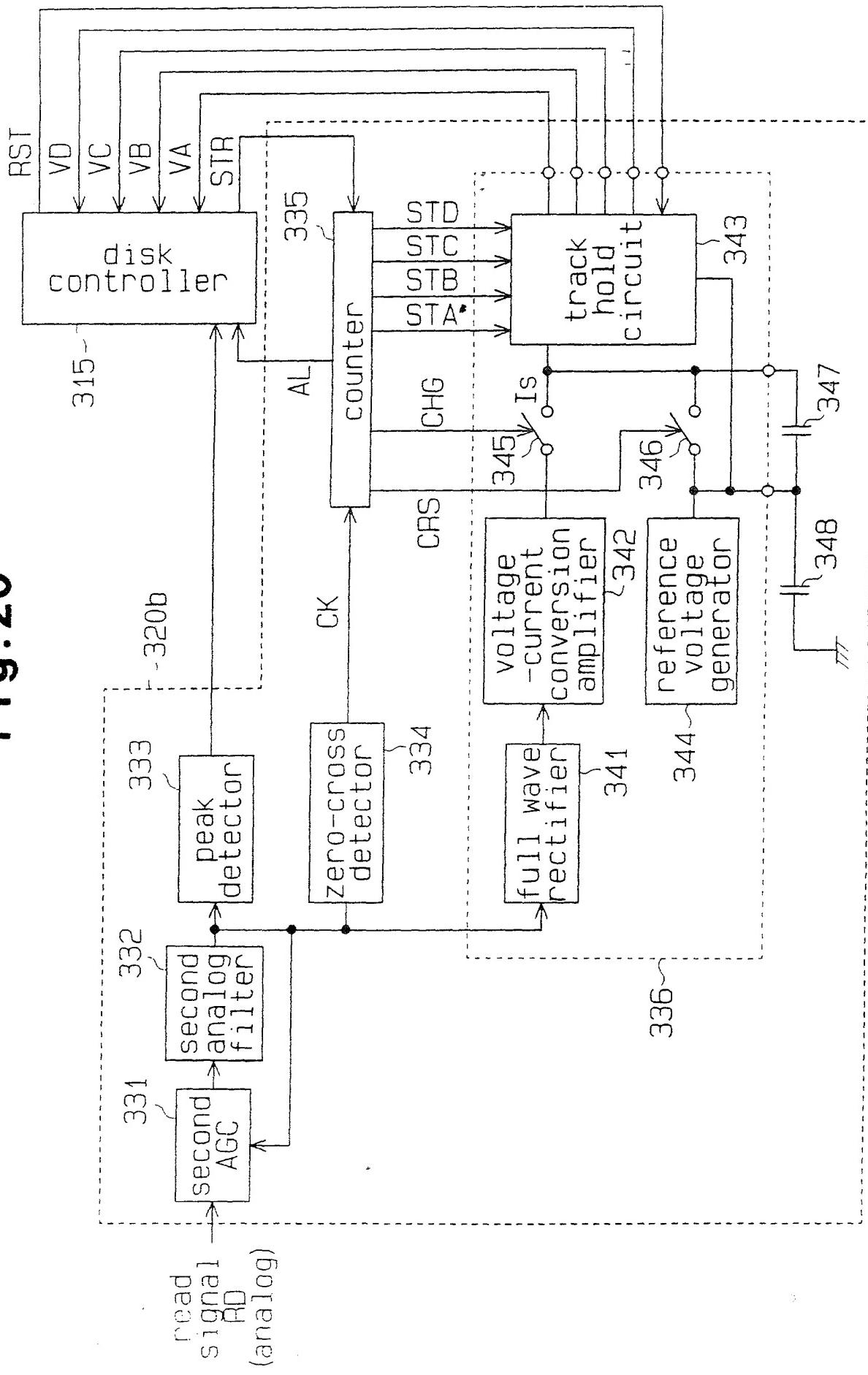


Fig. 21

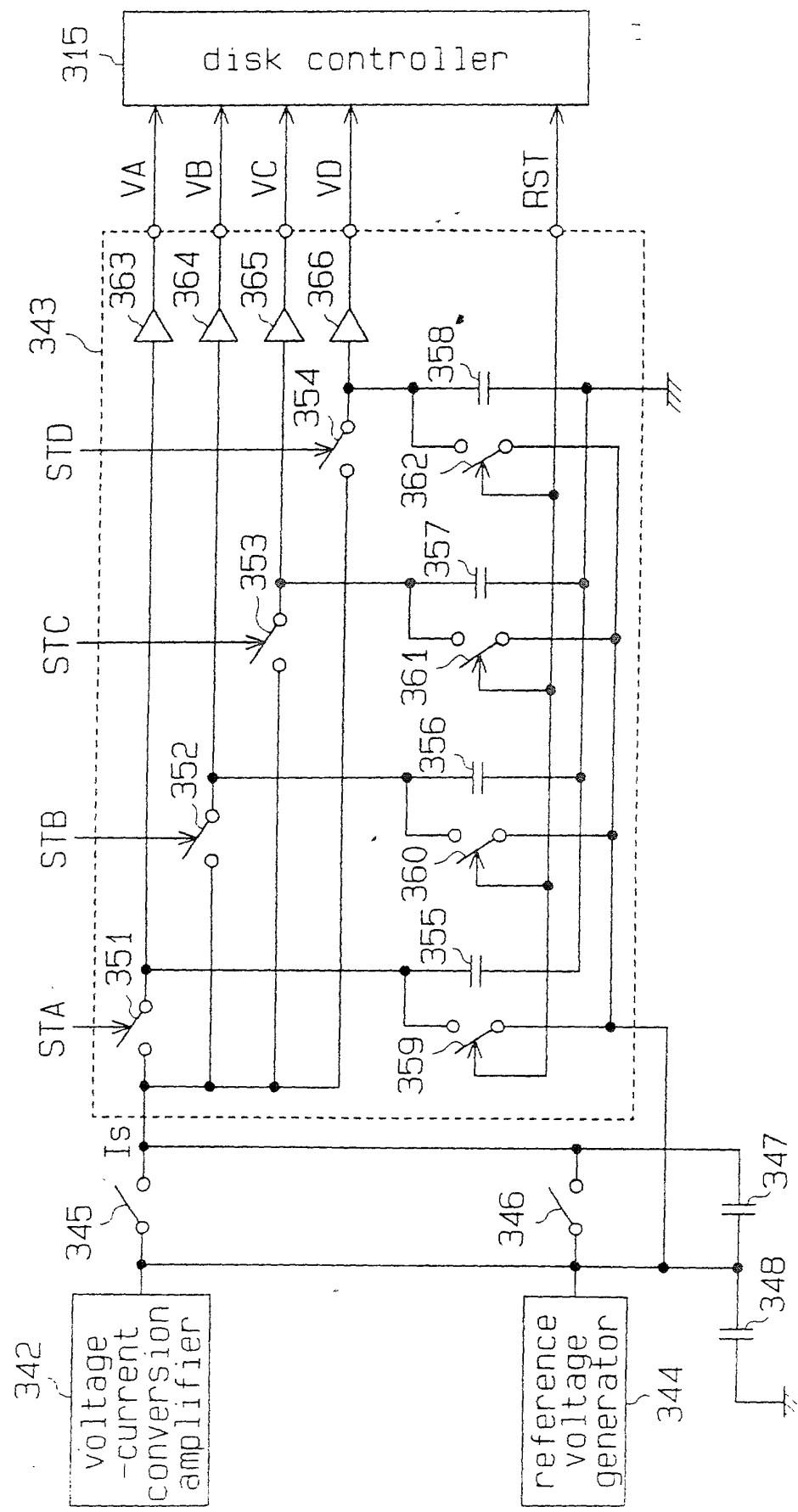


Fig.22

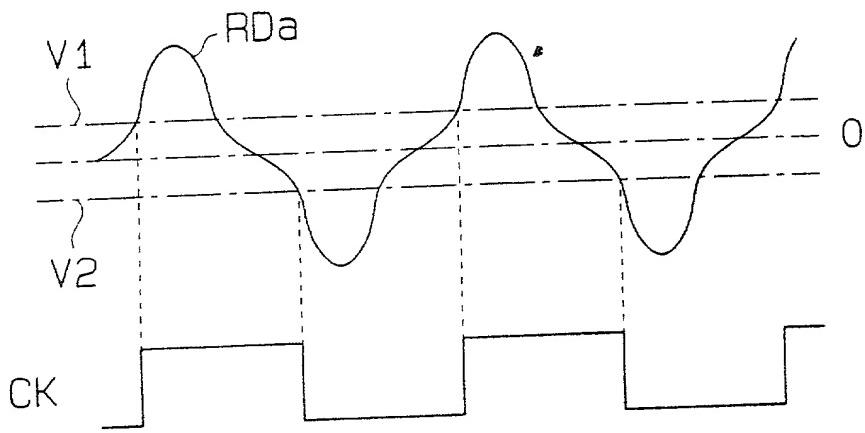


Fig. 23

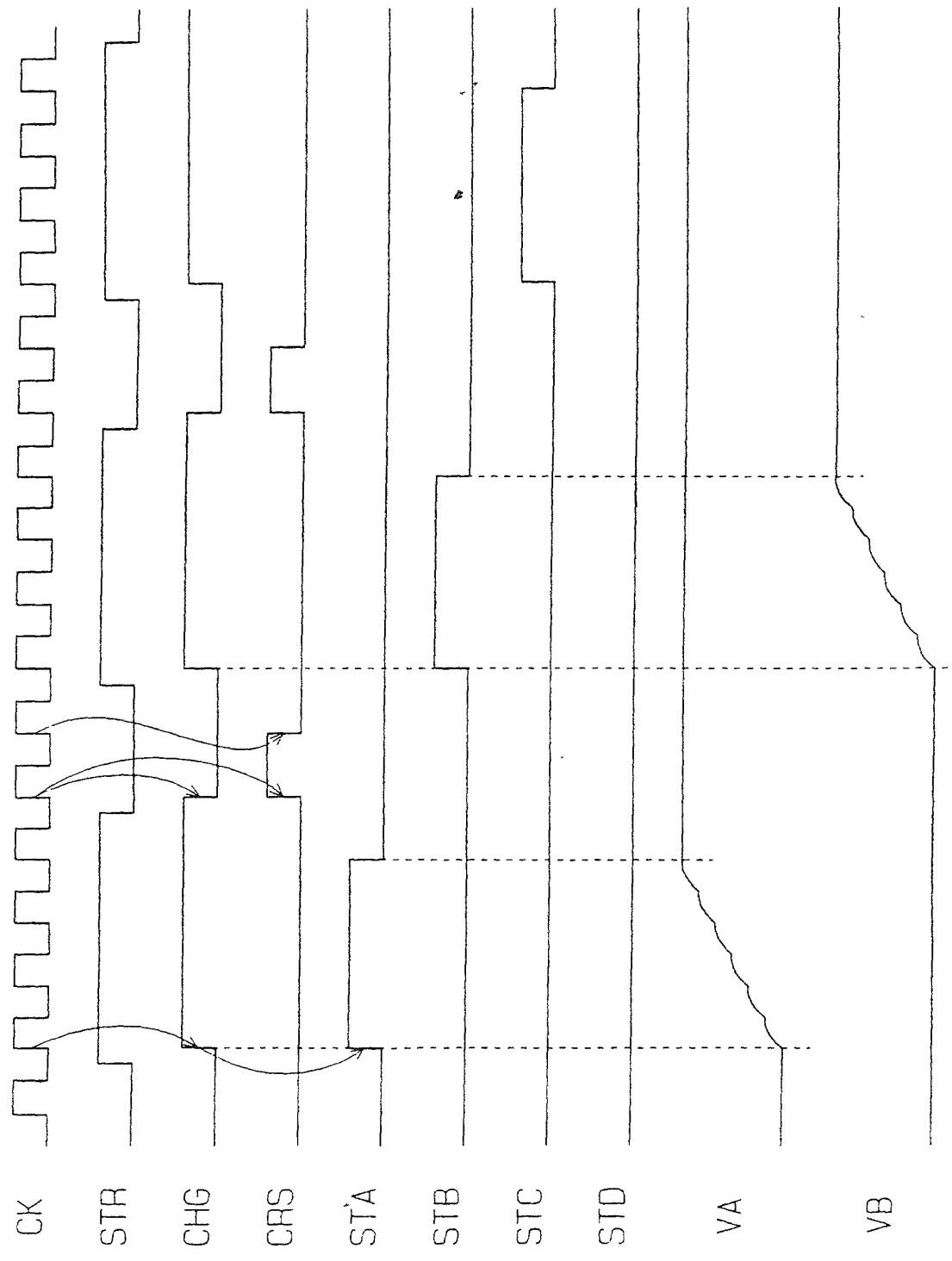


Fig. 24

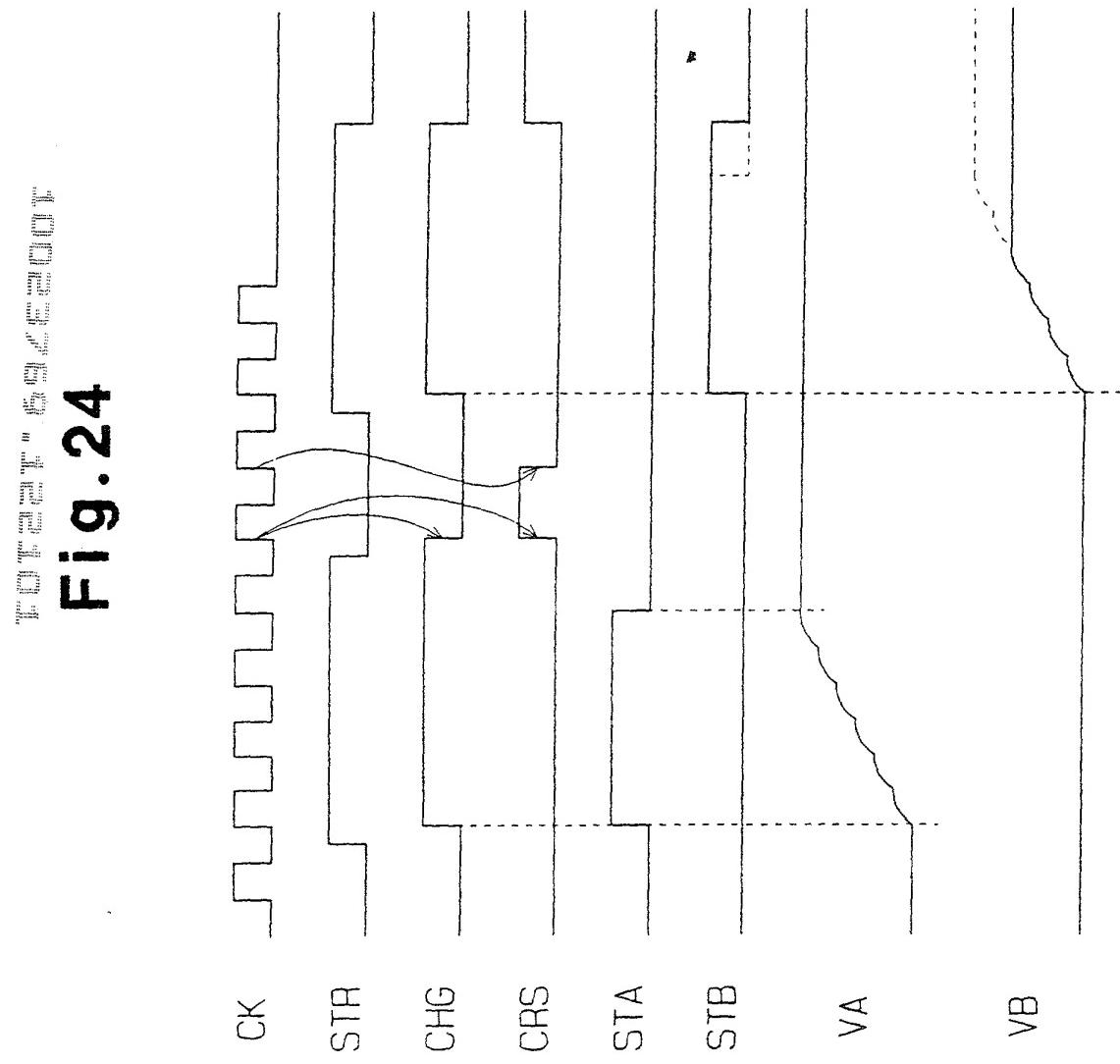


Fig. 25

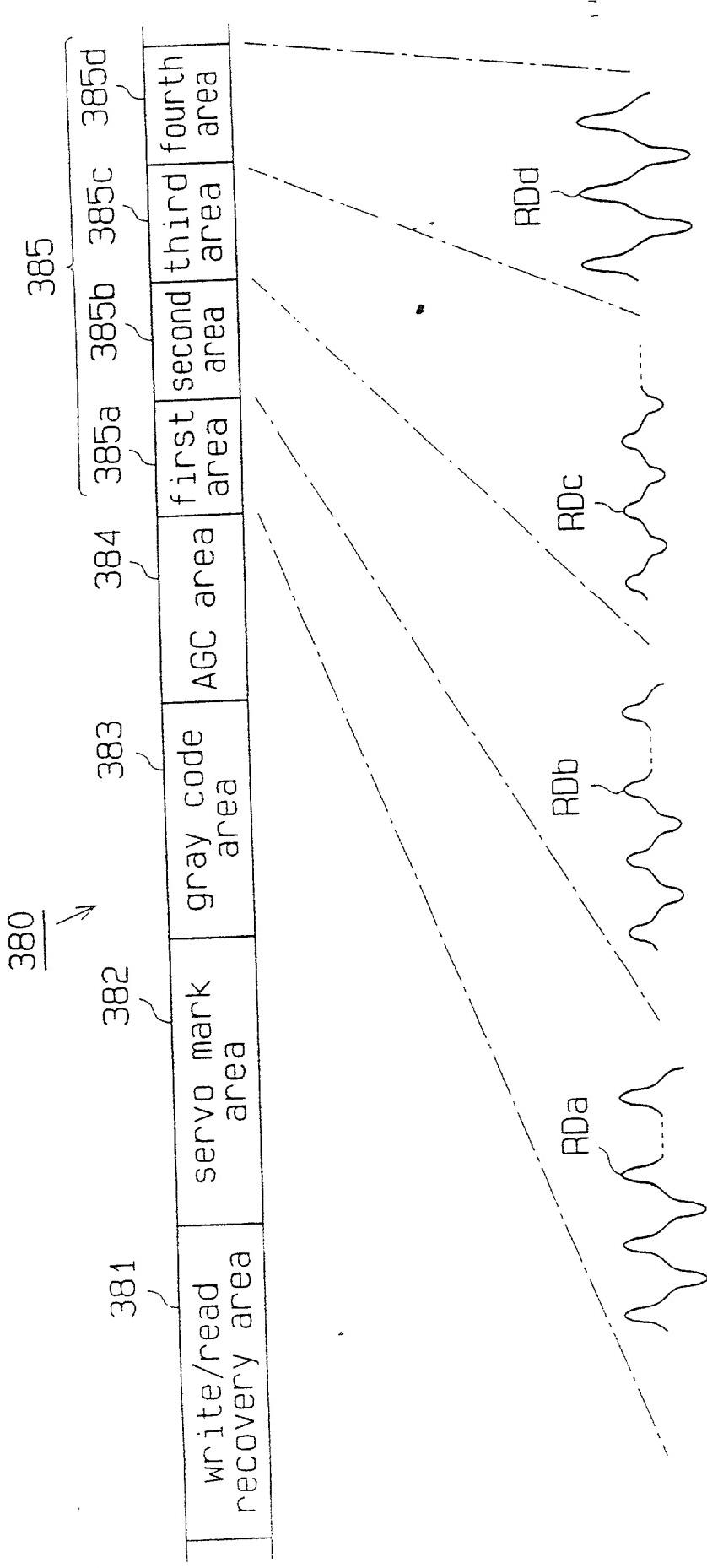


Fig. 26

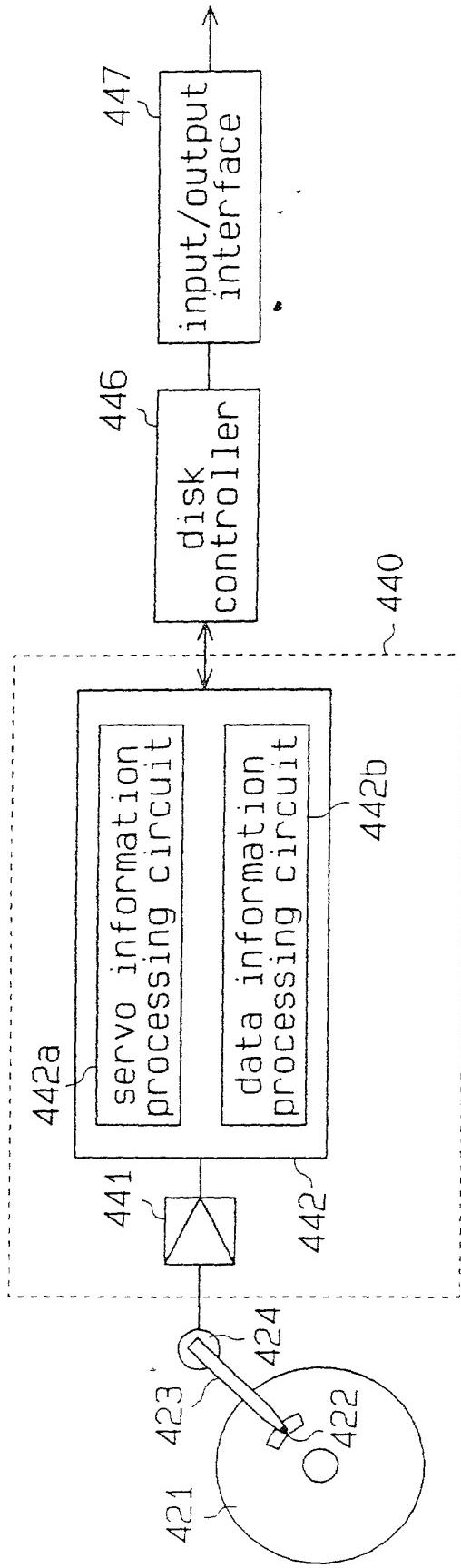


Fig. 27

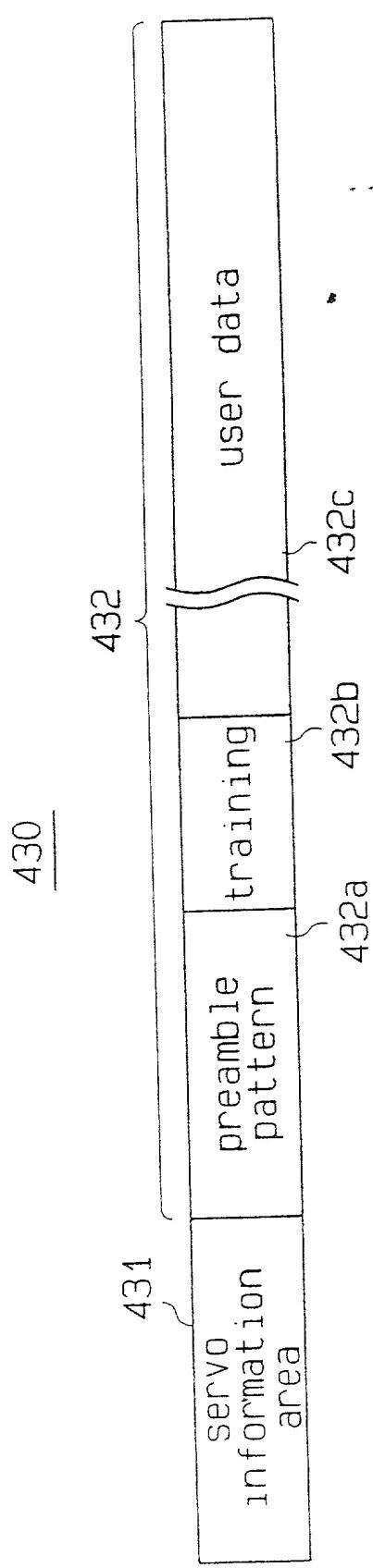


Fig. 28

DISK CONTROLLER CIRCUIT

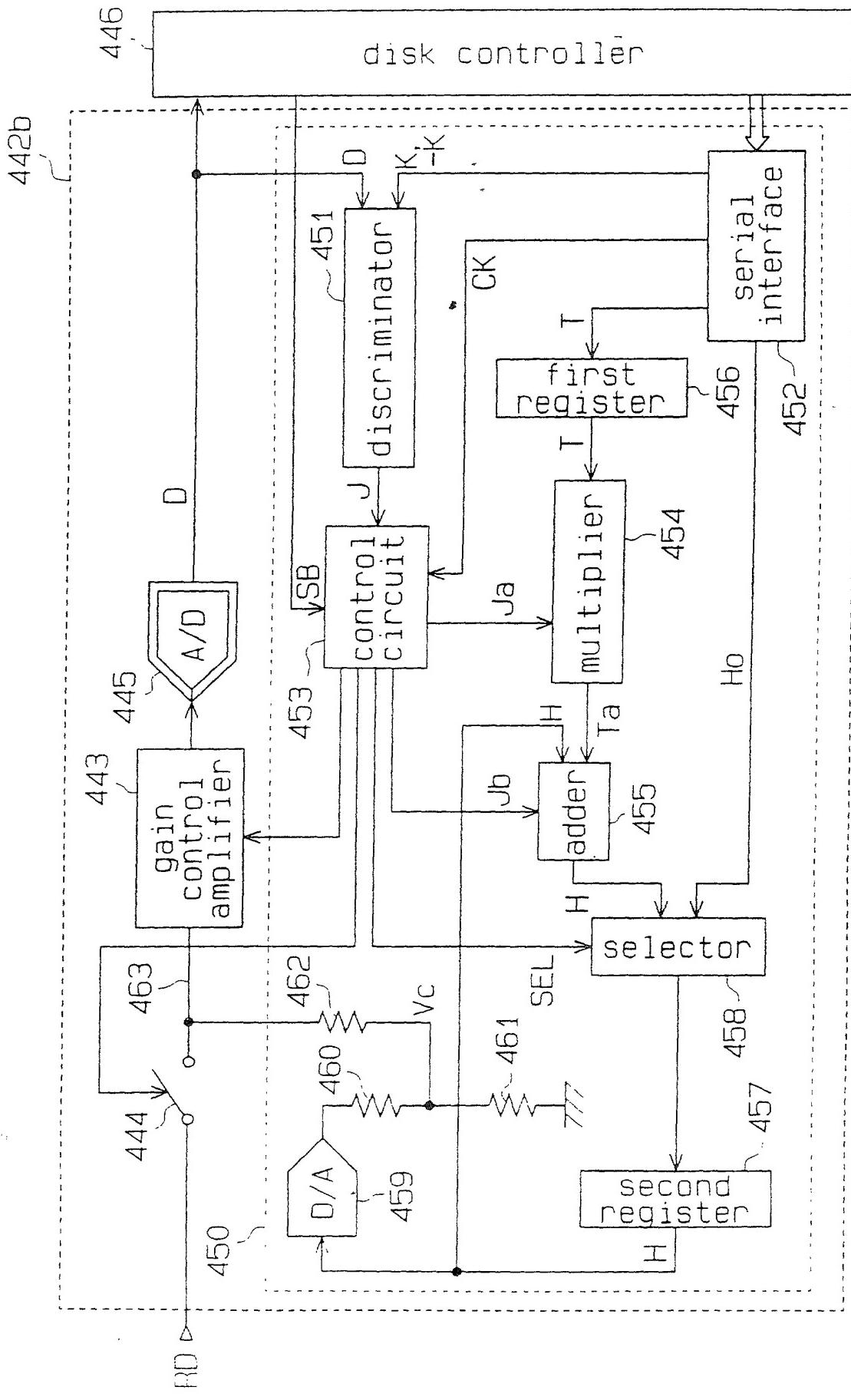


Fig. 29

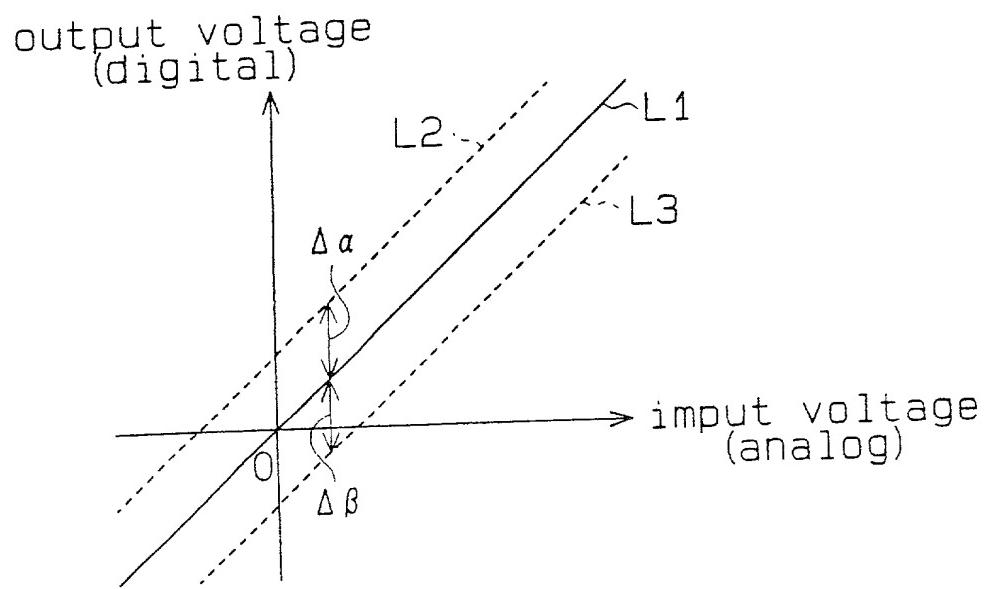


Fig. 30

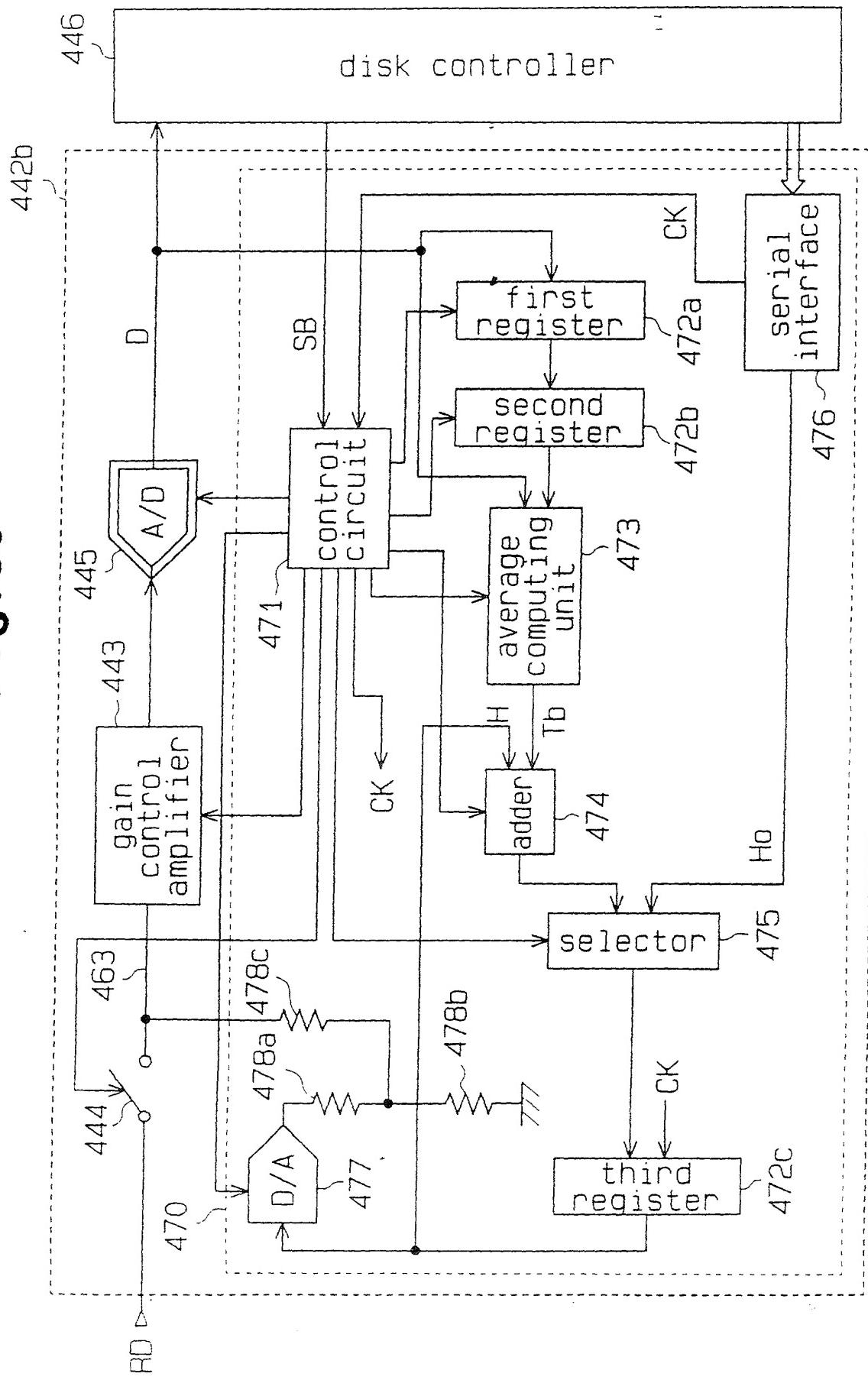


Fig. 31

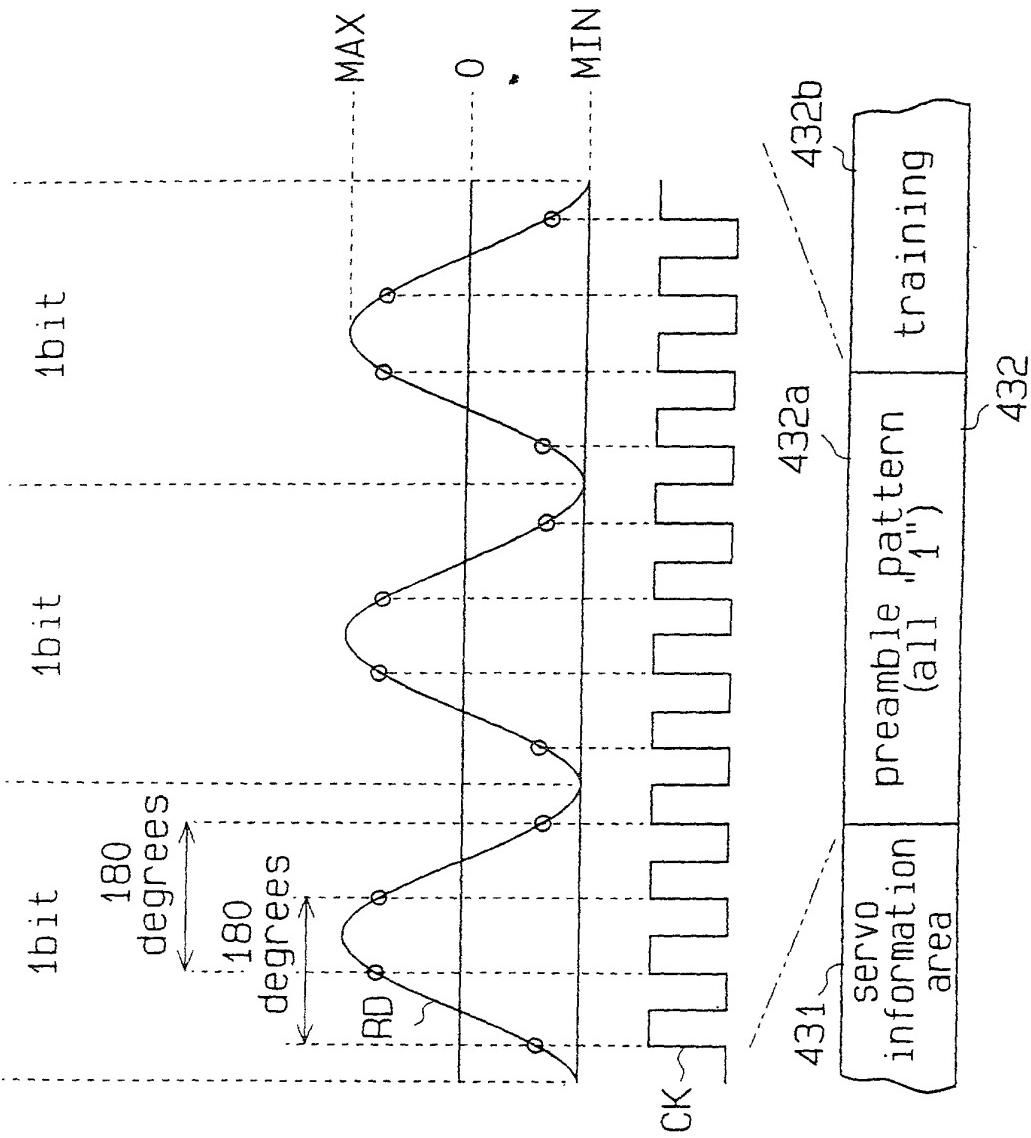


Fig. 32

图 32 是一个数字信号处理和锁相环 (PLL) 结构的框图。

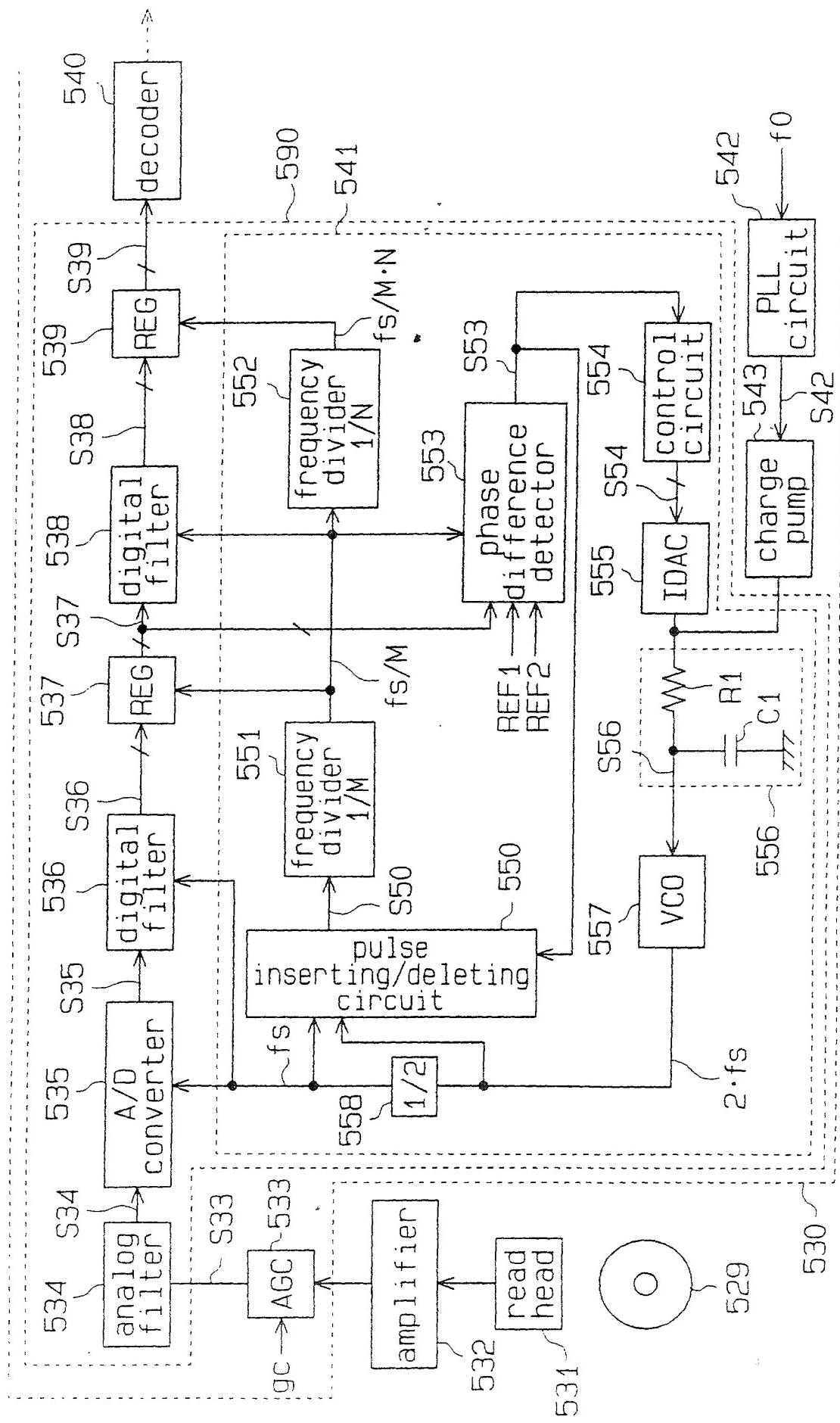


Fig. 33

REF1
REF2

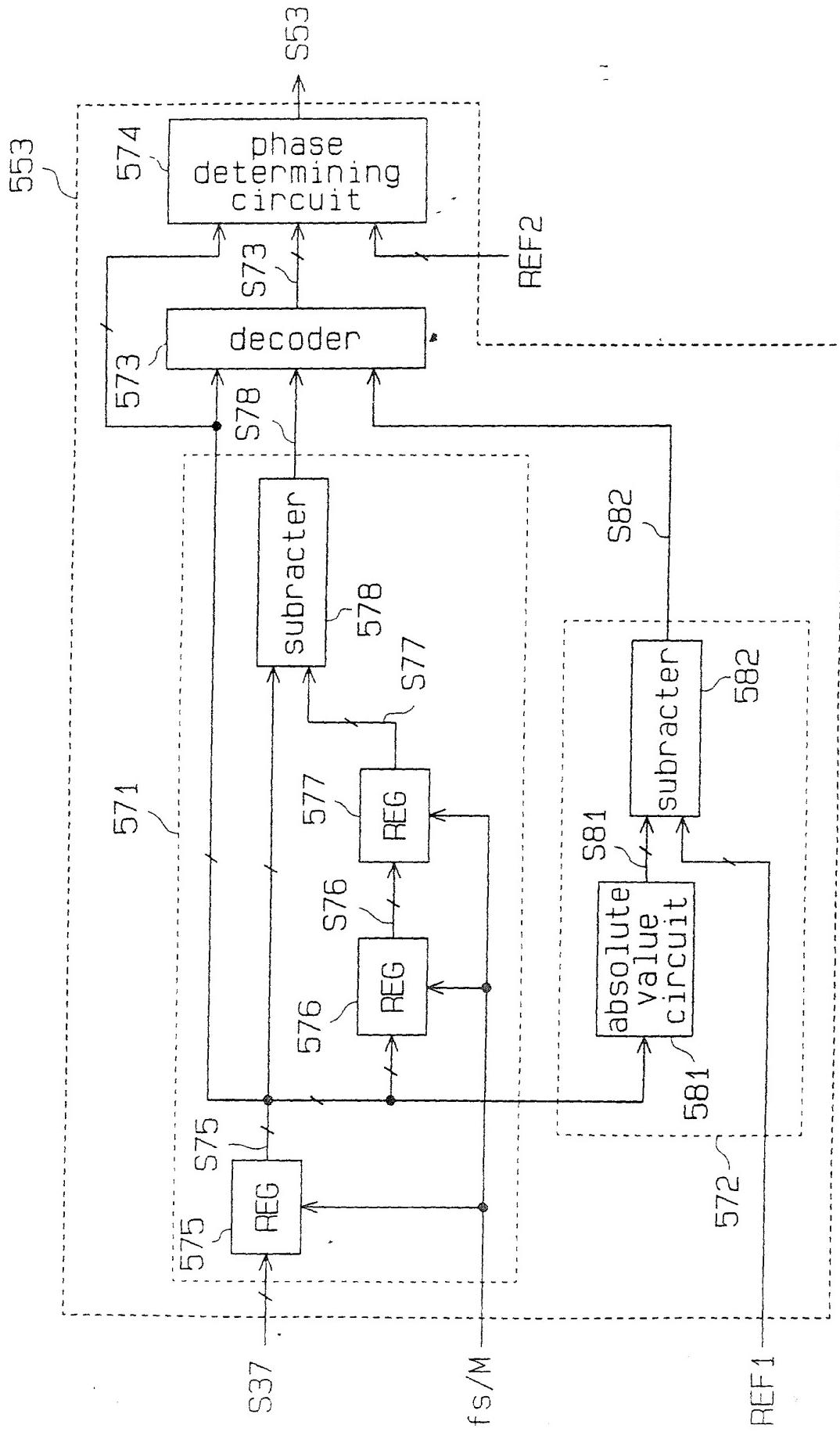


Fig.34A

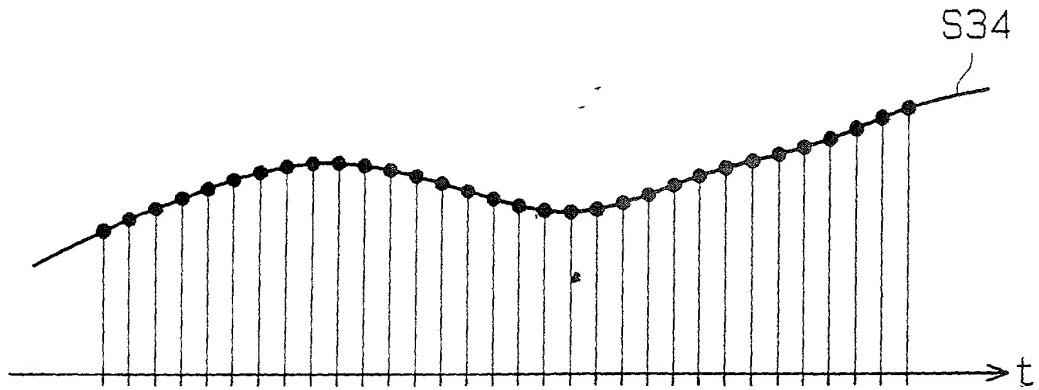


Fig.34B

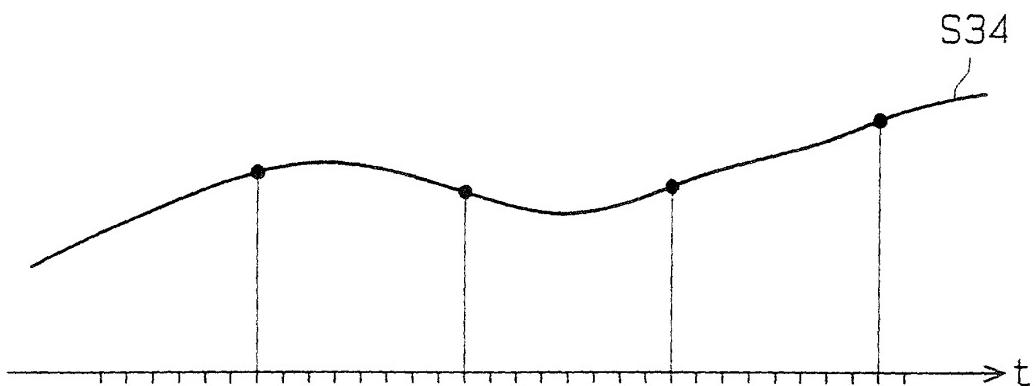


Fig.34C

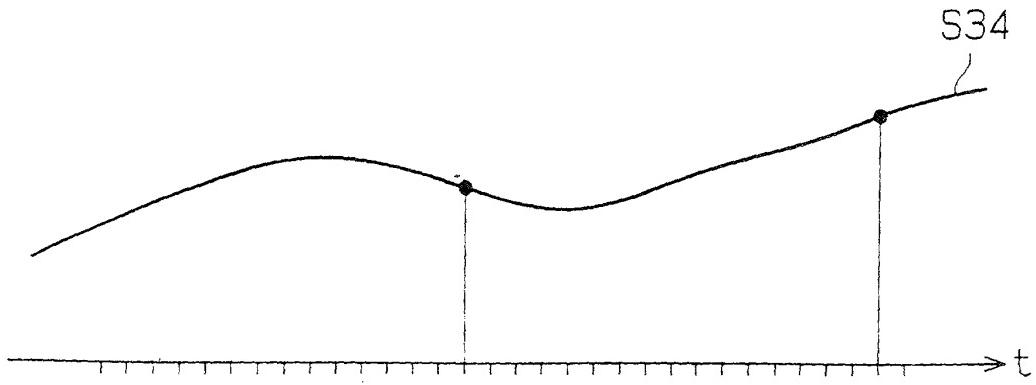


Fig. 35

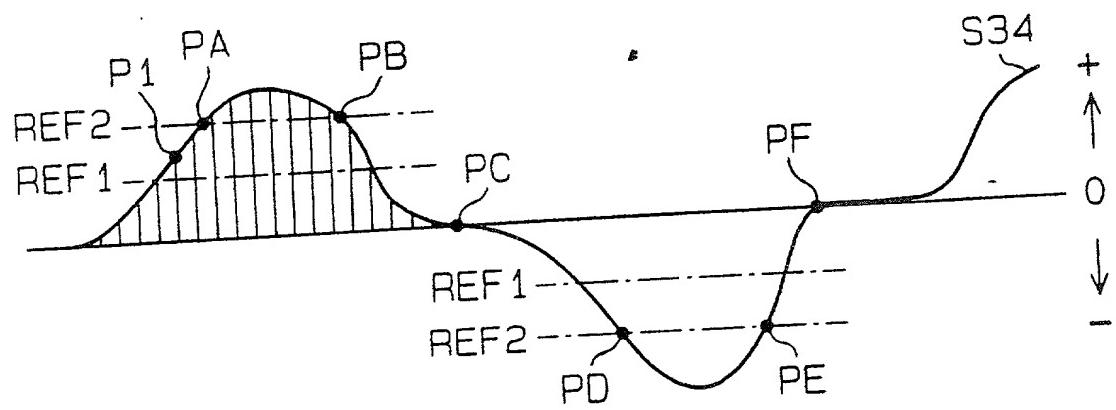


Fig. 36

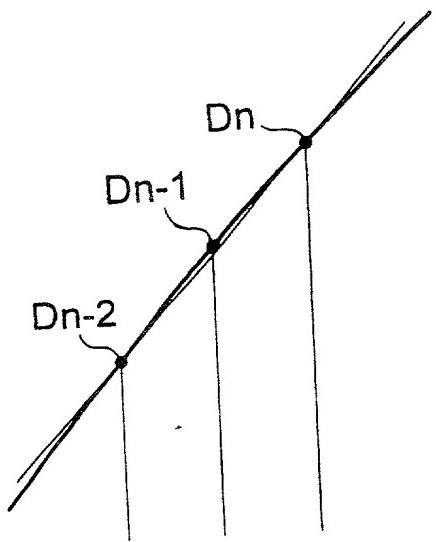


Fig.37

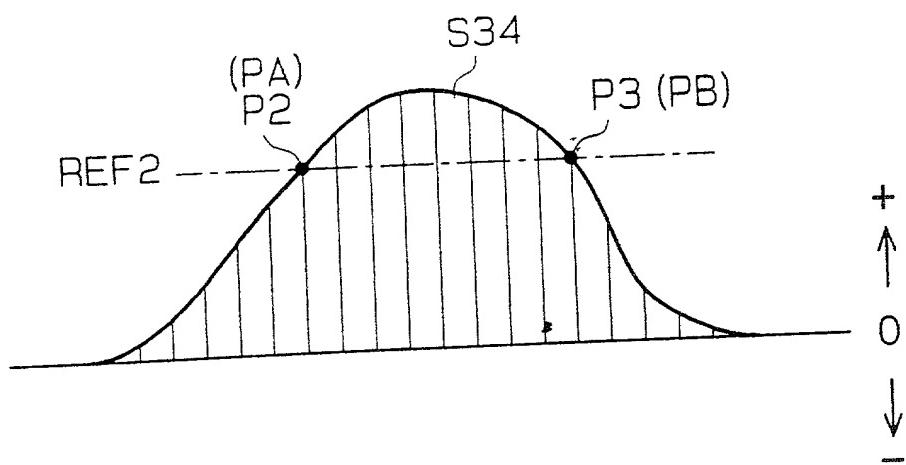


Fig.38

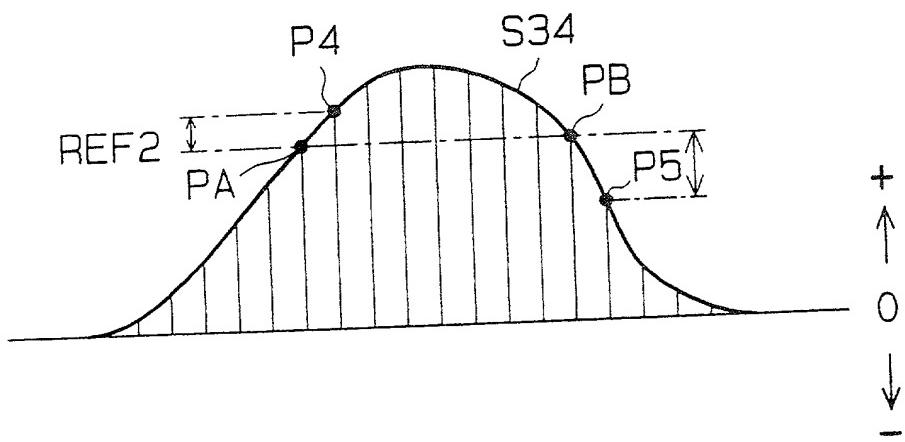


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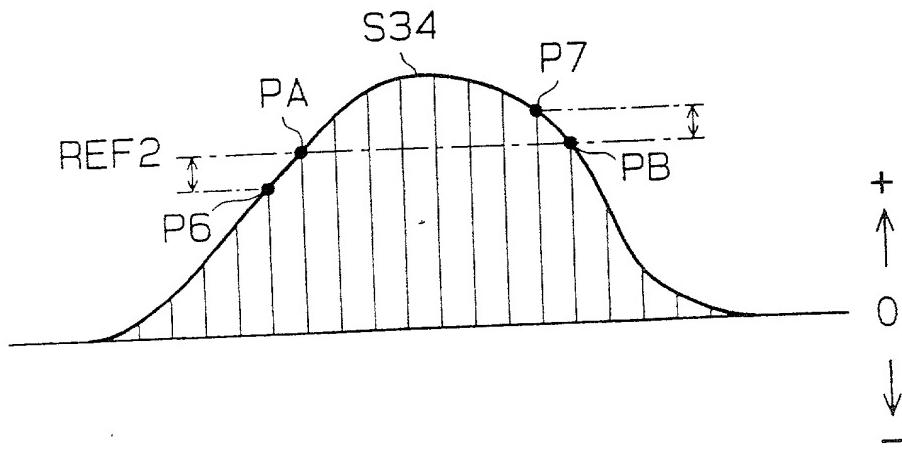


Fig. 40A

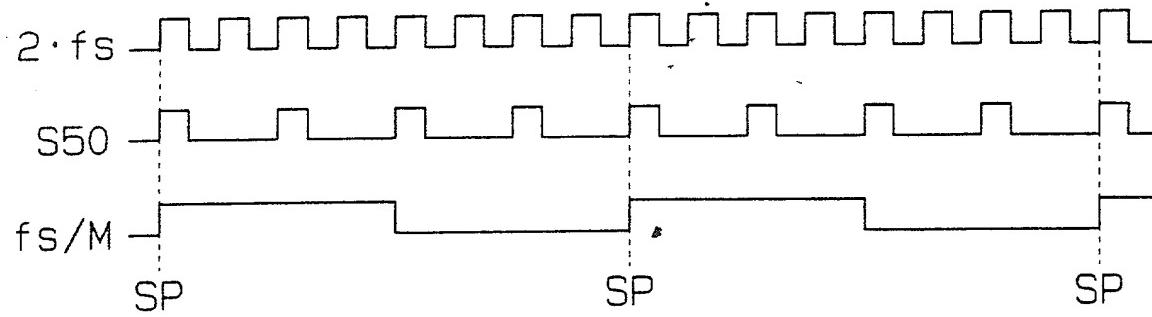


Fig. 40B

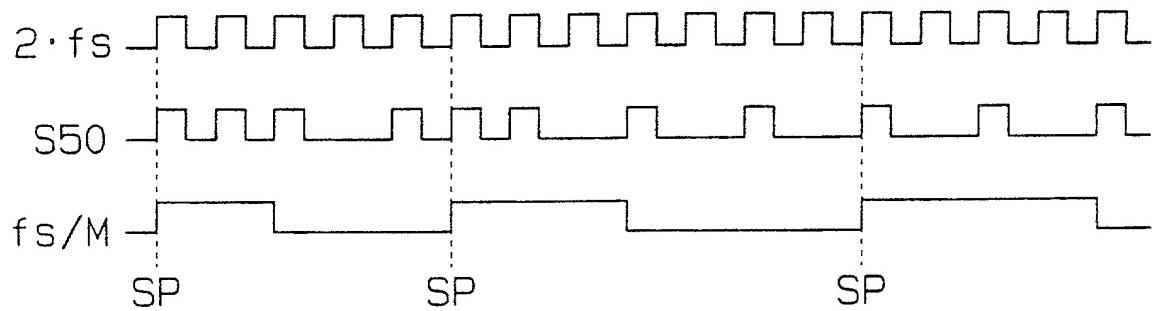


Fig. 40C

